State of Multicore OCaml

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Outline

- Overview of the multicore OCaml project
- Multicore OCaml runtime design
- Future directions

Multicore OCaml

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- Add native support for concurrency and (shared-memory) parallelism to OCaml

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- History
  - ★ Jan 2014: Initiated by Stephen Dolan and Leo White
  - ★ Sep 2014: Multicore OCaml design @ OCaml workshop
  - ★ Jan 2015: KC joins the project at OCaml Labs
  - ★ Sep 2015: Effect handlers @ OCaml workshop
  - ★ Jan 2016: Native code backend for Amd64 on Linux and OSX
  - ★ Jun 2016: Multicore rebased to 4.02.2 from 4.00.0
  - ★ Sep 2016: Reagents library, *Multicore backend for Links* @ OCaml workshop
  - ★ Apr 2017: ARM64 backend

Multicore OCaml

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  - ★ Jun 2017: Handlers for Concurrent System Programming @ TFP
  - ★ Sep 2017: Memory model proposal @ OCaml workshop
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  - ★ Jun 2018: Memory model @ PLDI
- Looking forward…
  - ★ Q3'18 — Q4'18: Implement missing features, upstream prerequisites to trunk
  - ★ Q1'19 — Q2'19: Submit feature-based PRs to upstream

Components

Multicore Runtime
+
Domains

Effect Handlers

Effect System

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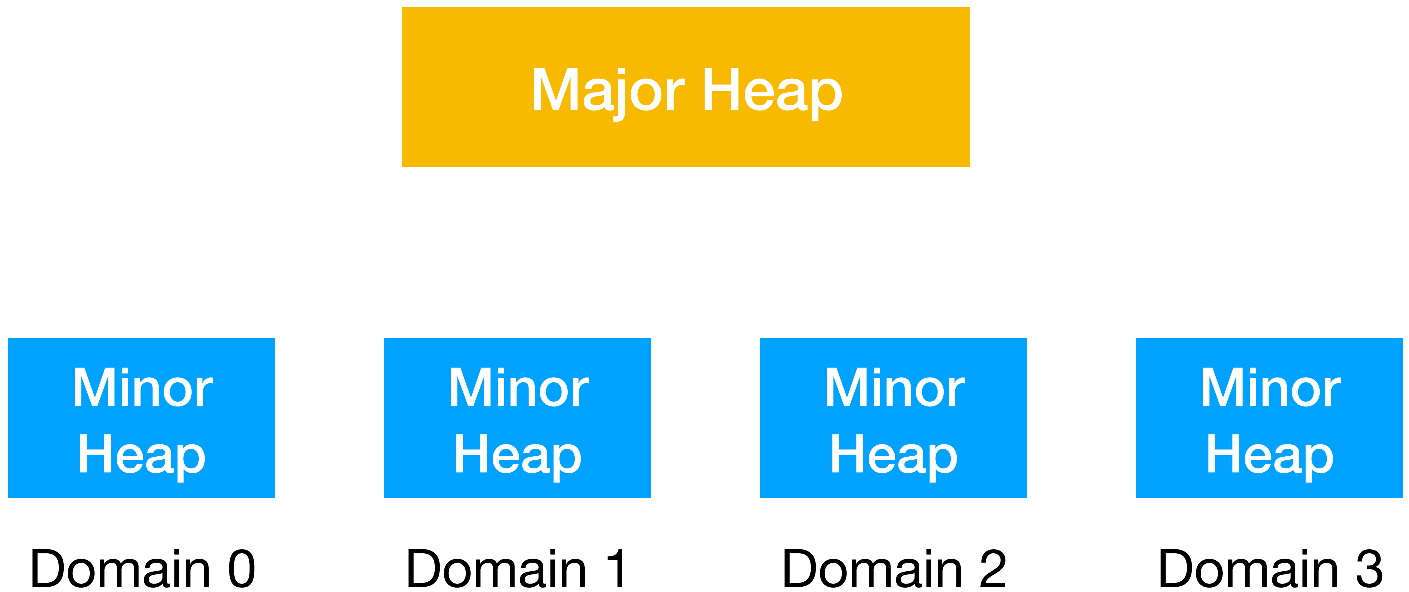
Multicore GC



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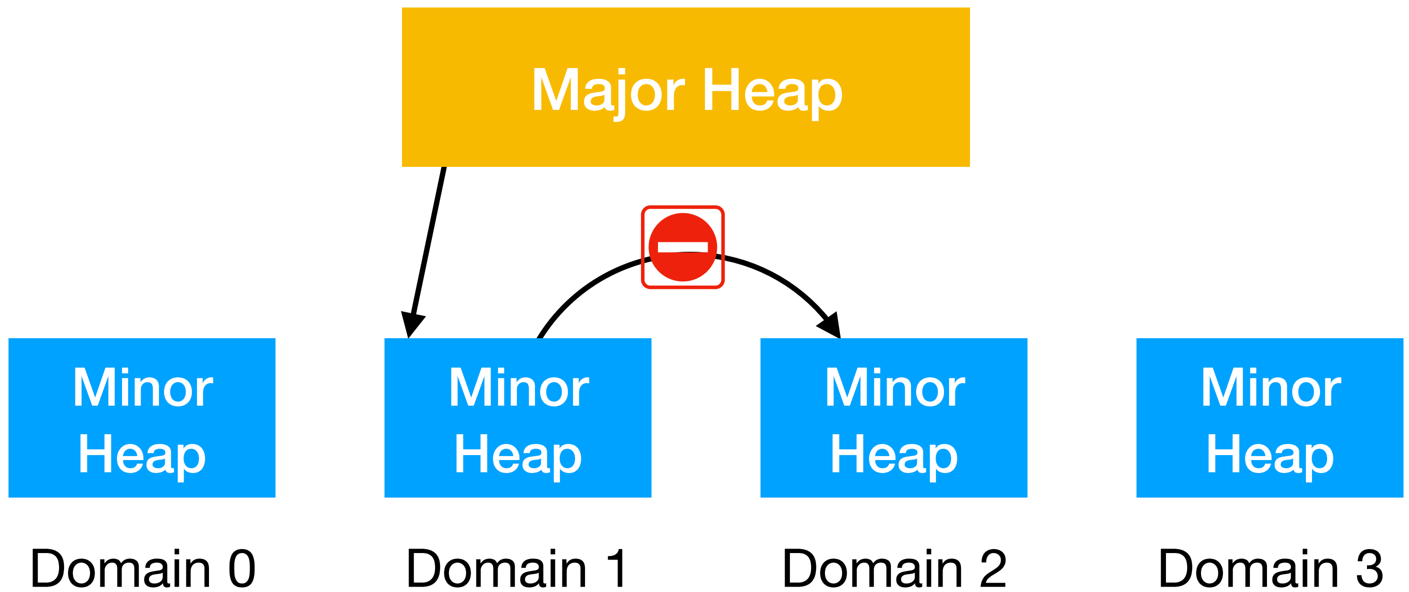

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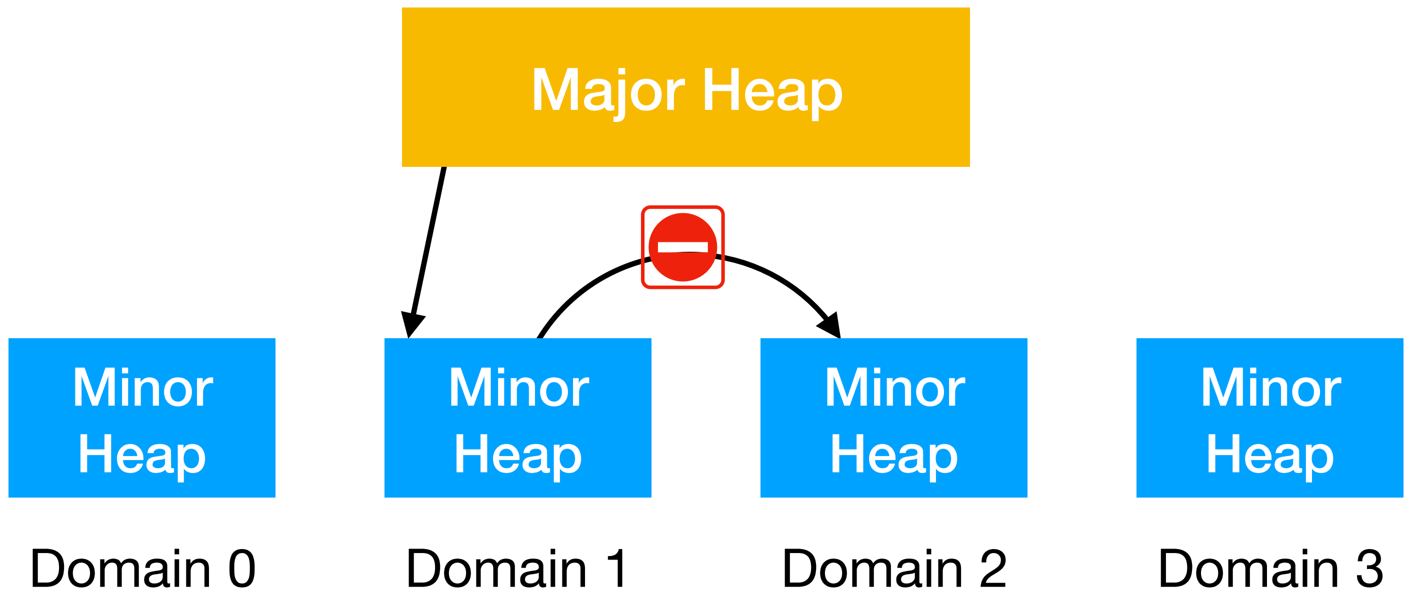

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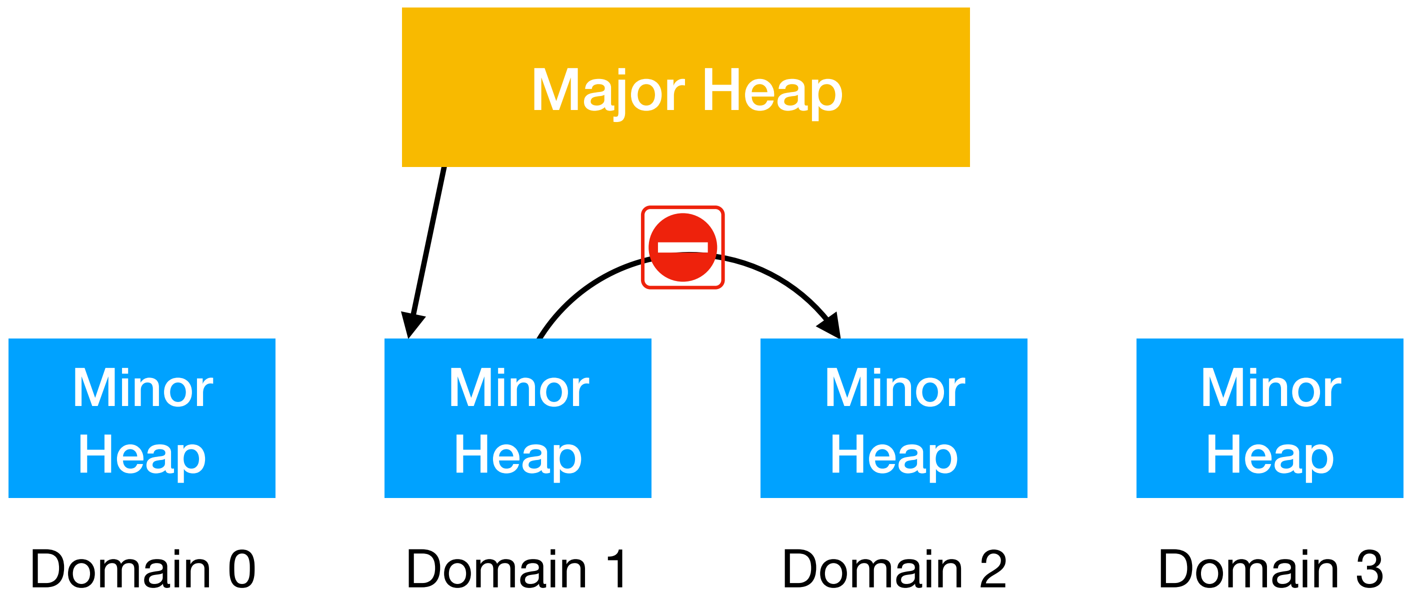

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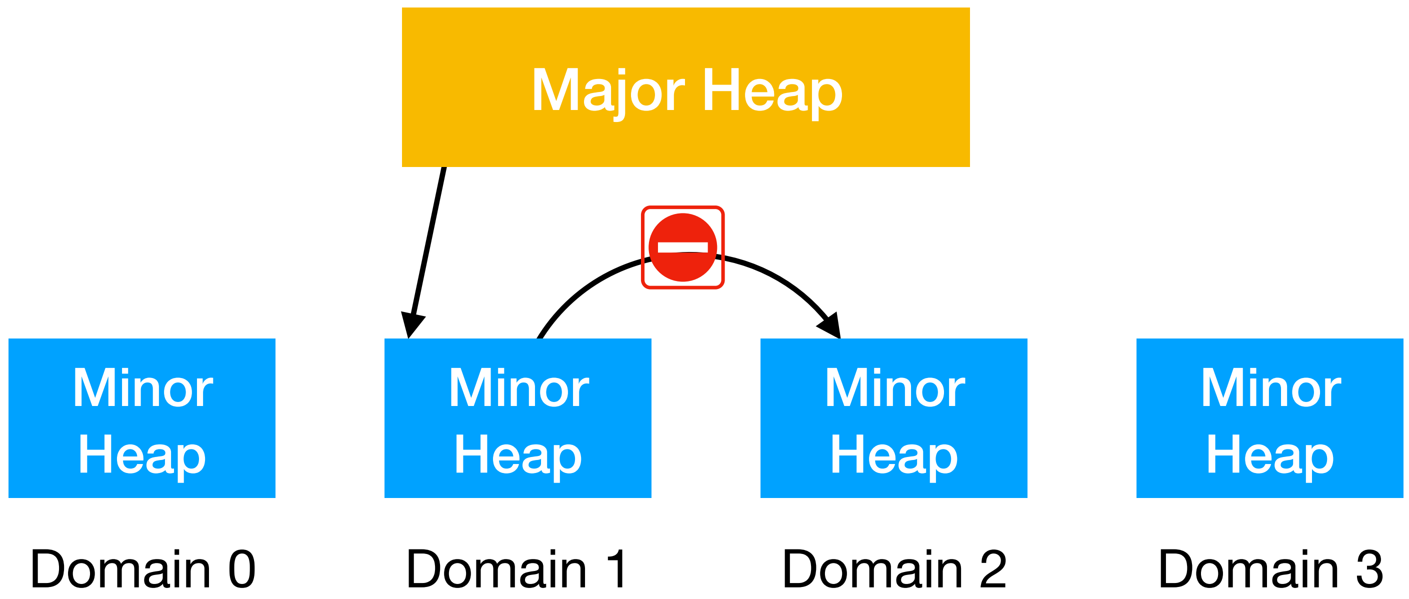

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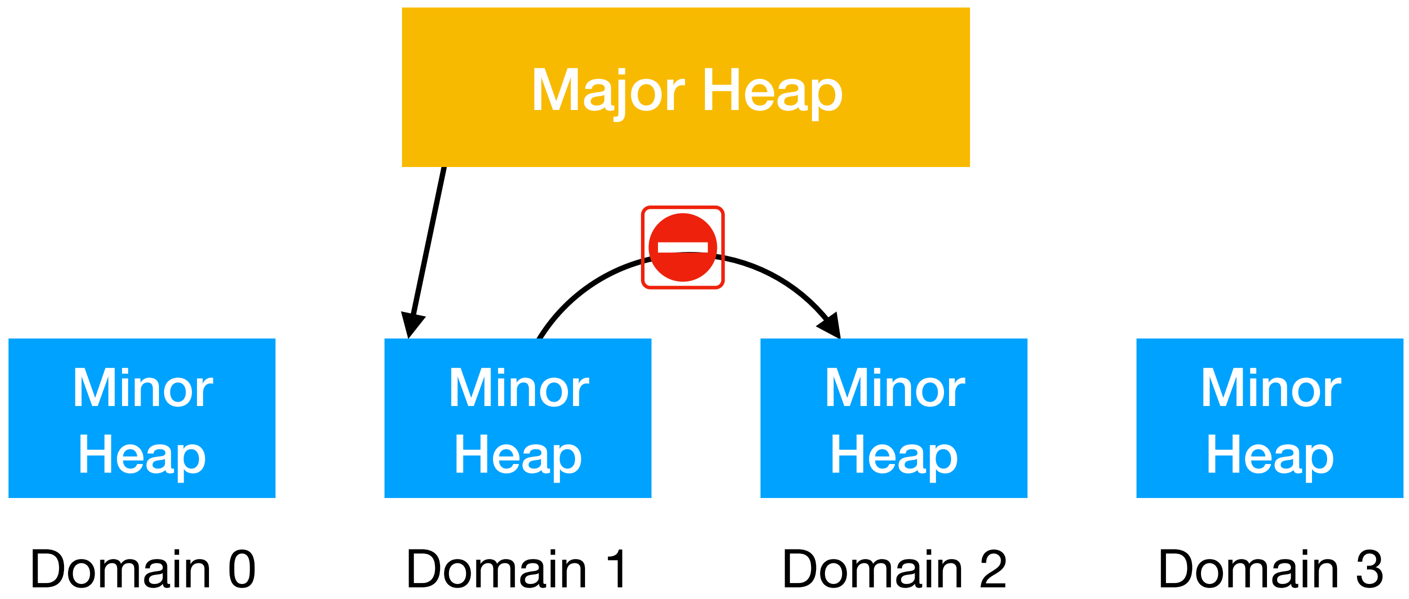

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- A new major GC based on VCGC [2] adapted to fibers, ephemerons, finalisers

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Major GC

- Concurrent, incremental, mark and sweep
  - ★ Uses deletion/yuasa barrier
  - ★ Upper bound on marking work per cycle (not fixed due to weak refs)
- 3 phases:
  - ★ Sweep-and-mark-main
  - ★ Mark-final
  - ★ Sweep-ephe

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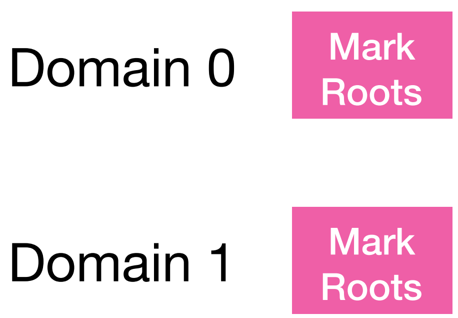

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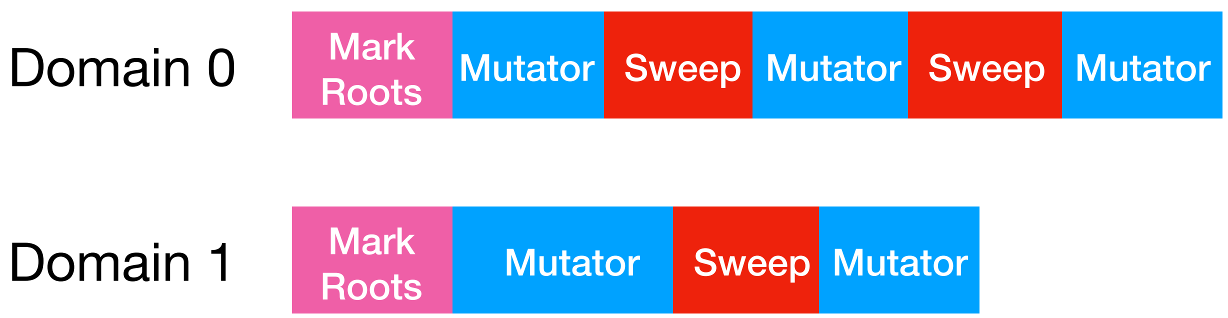

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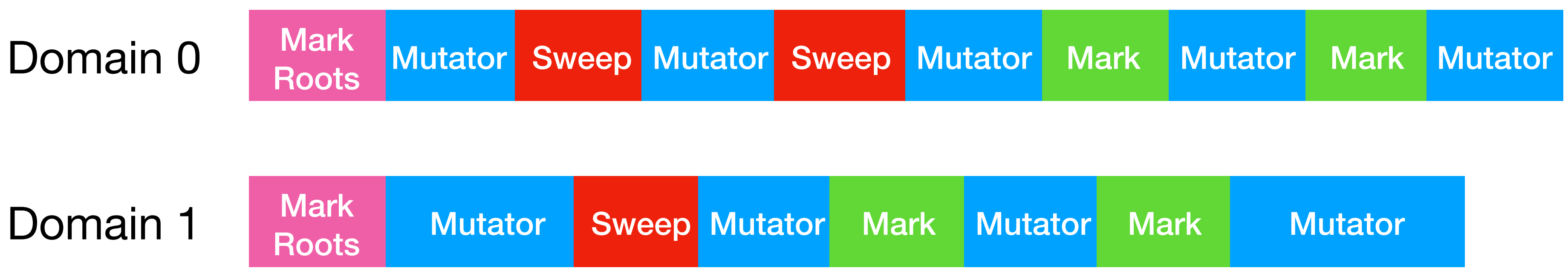

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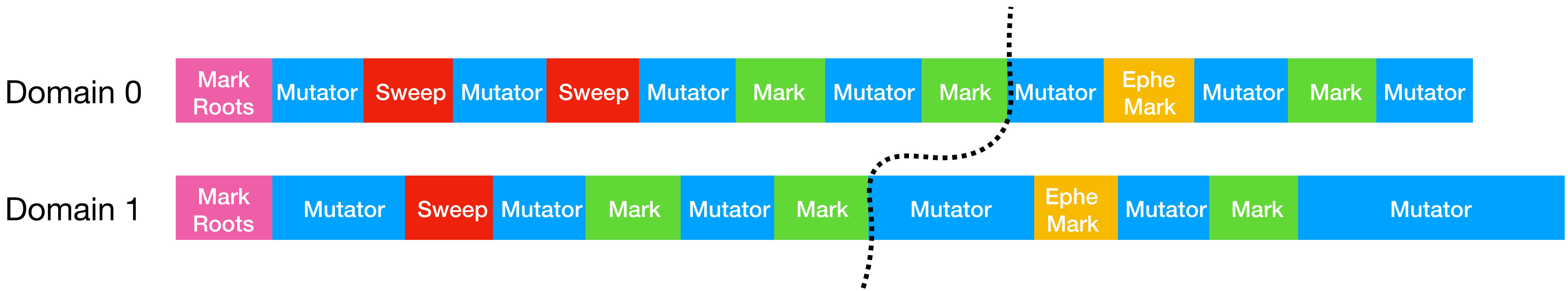

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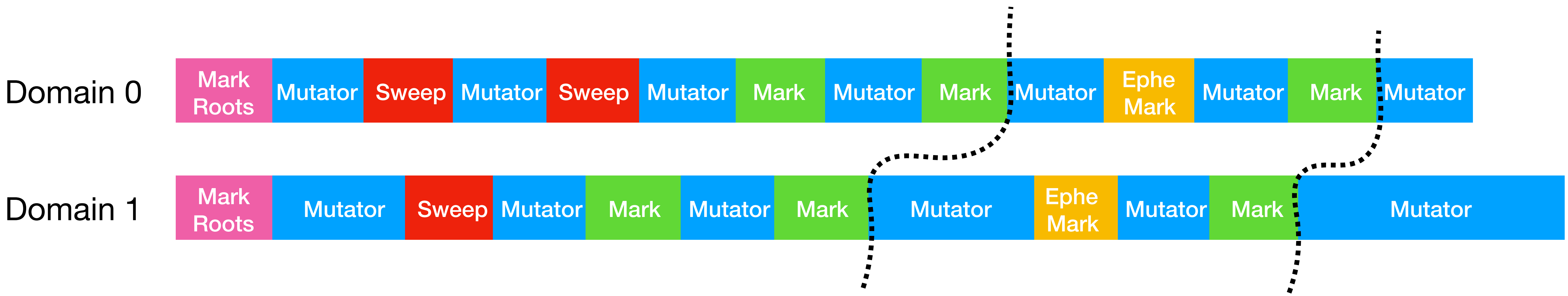

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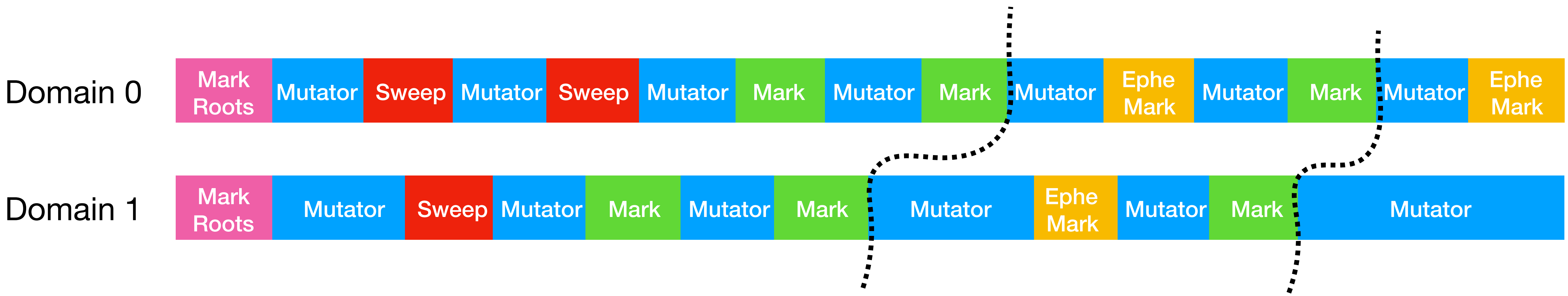

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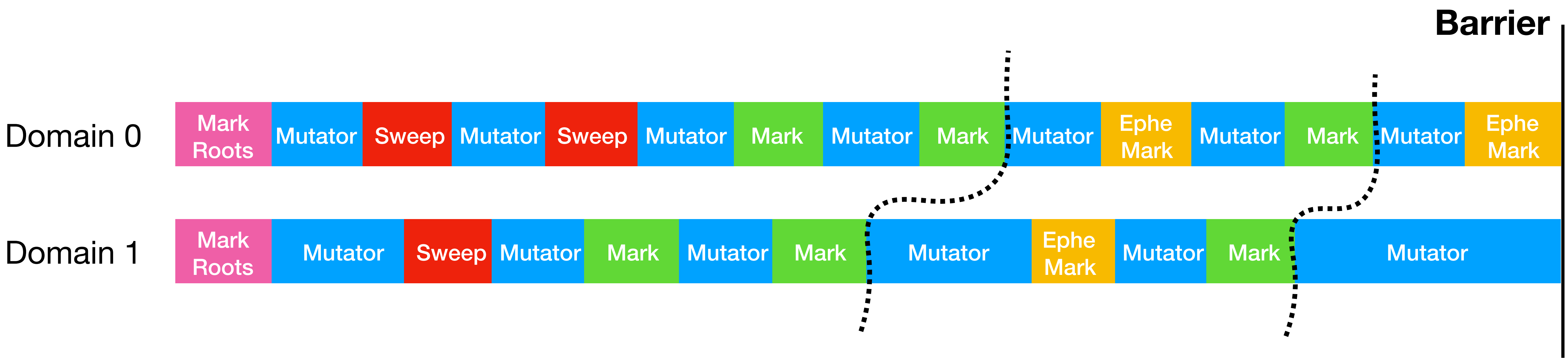

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- Global barrier to switch to the next phase
  - ★ Reading weak keys may make unreachable objects reachable
  - ★ Verify that the phase termination conditions hold

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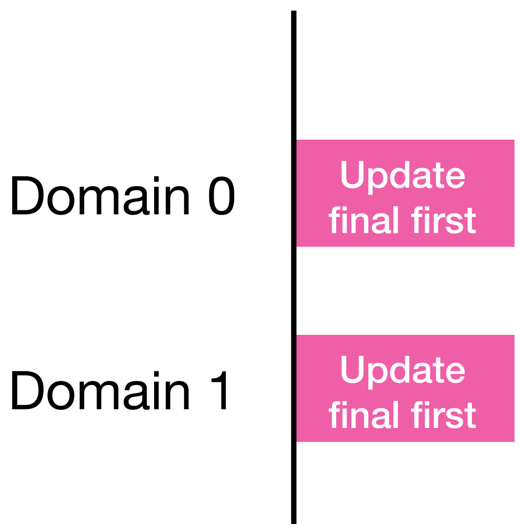

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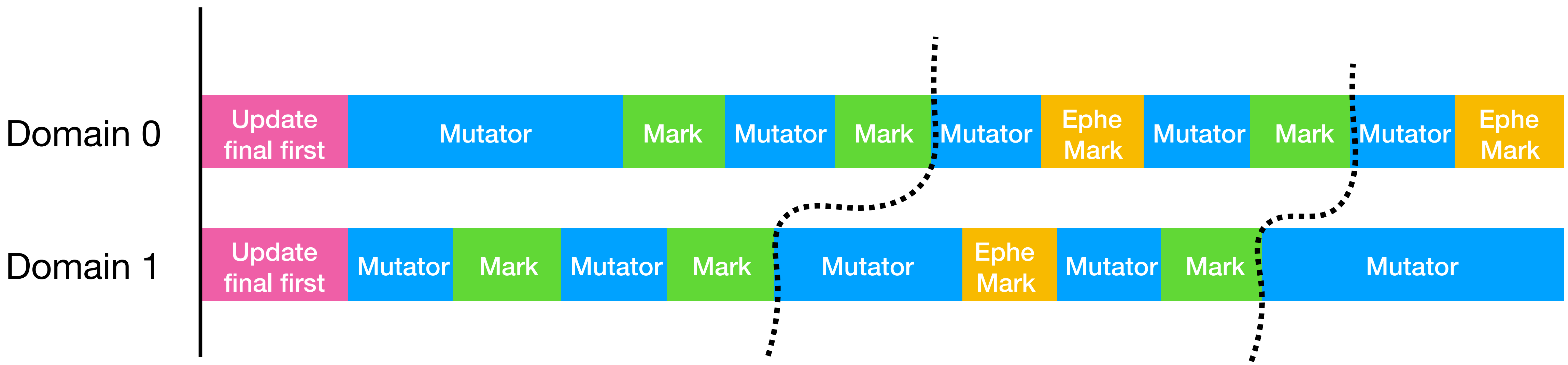

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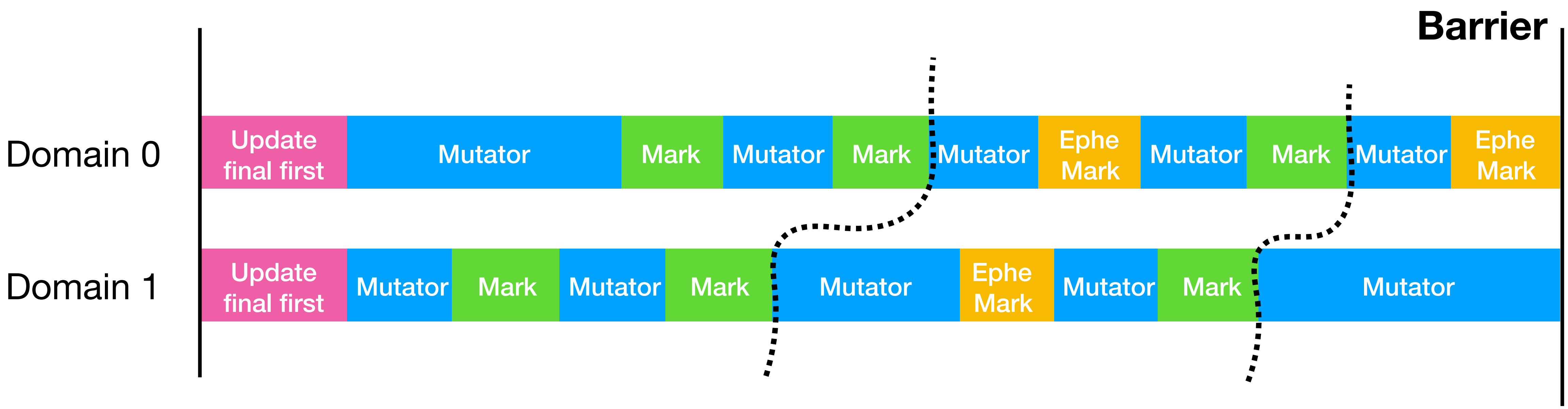

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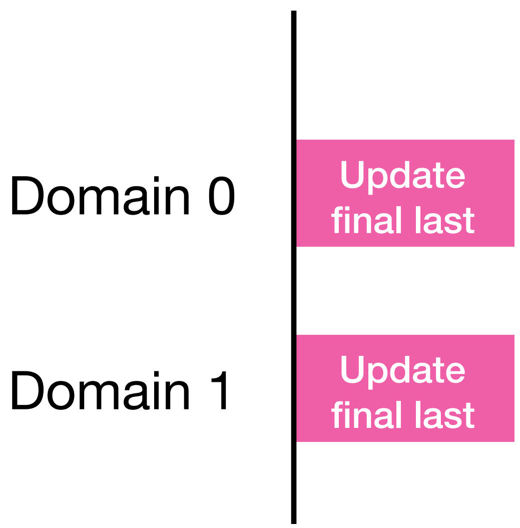

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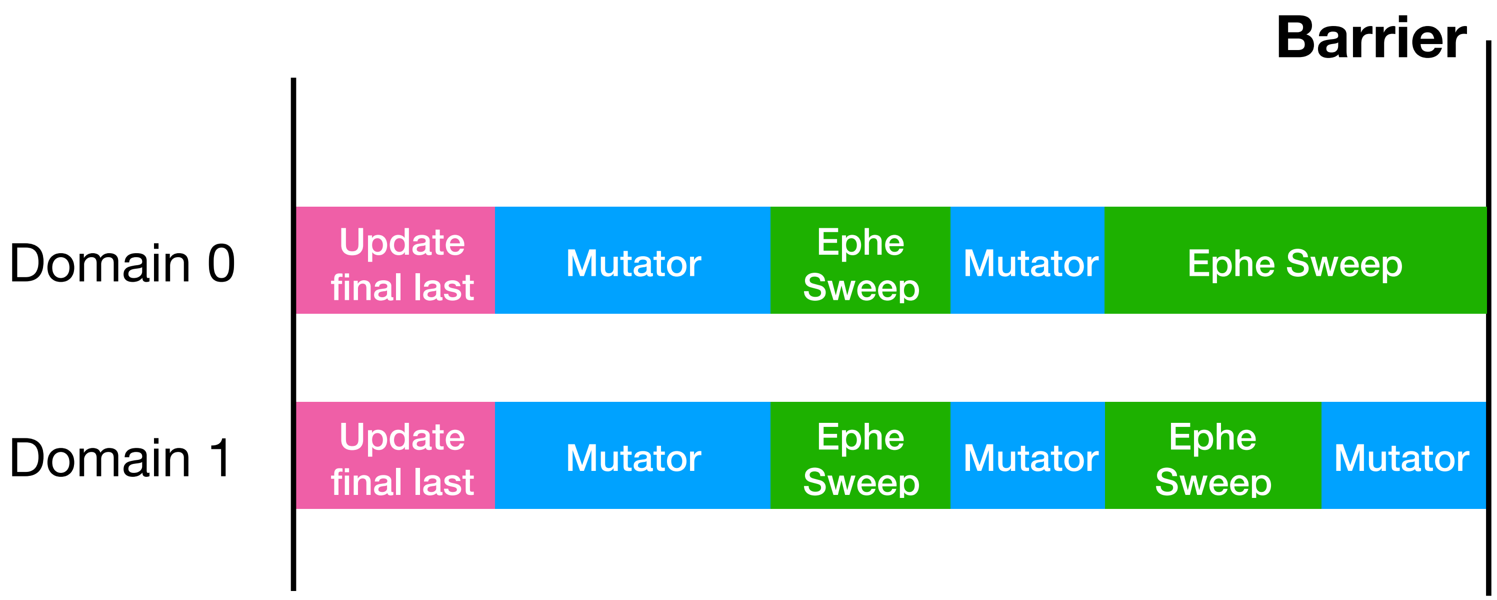

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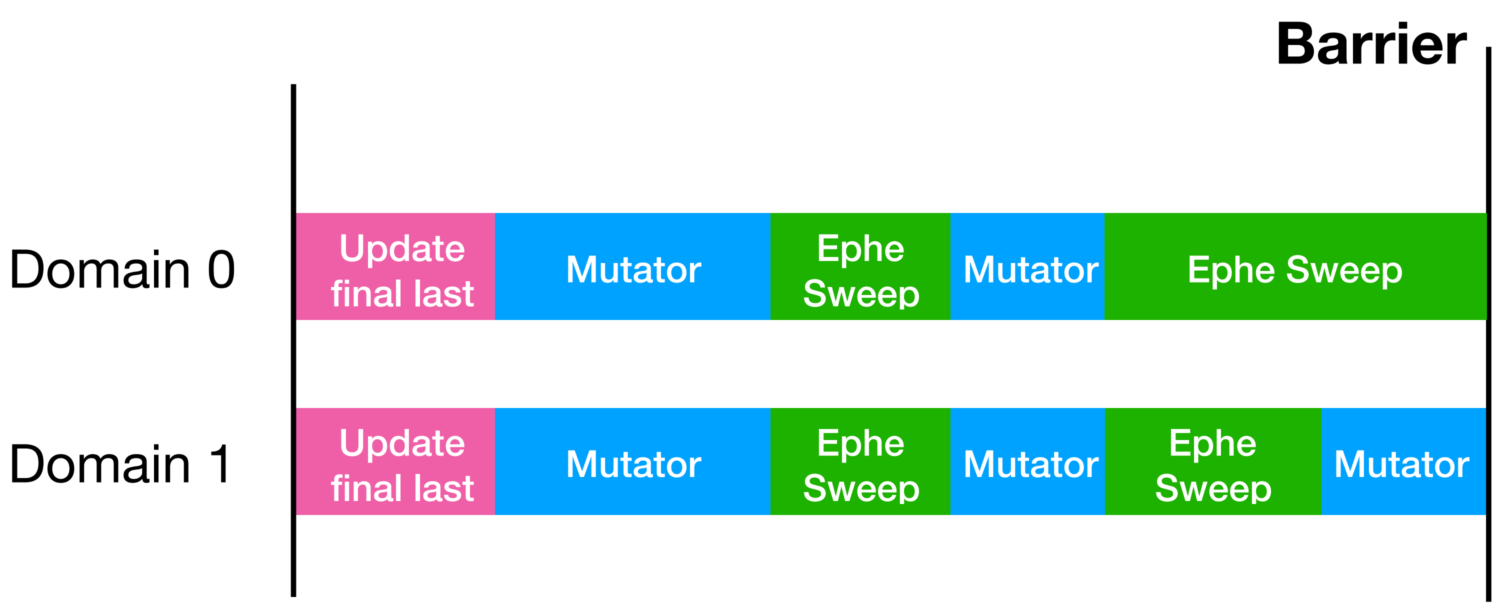

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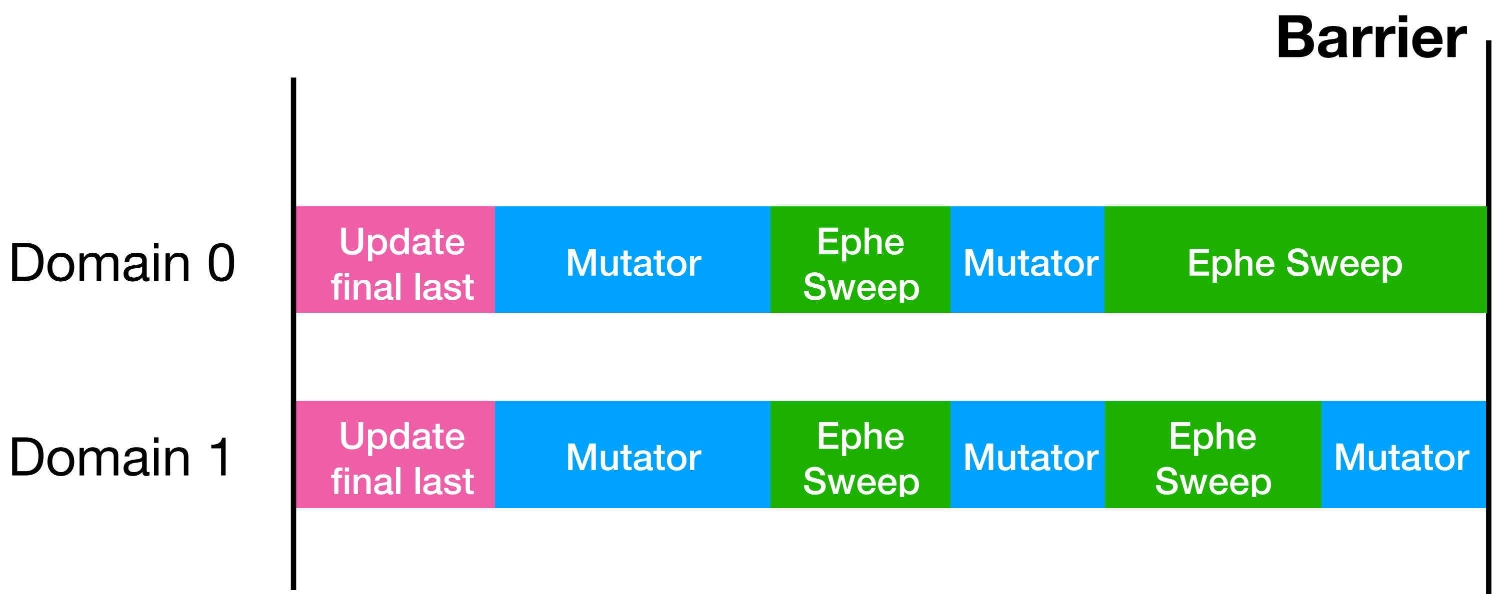

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- Major GC algorithm verified in SPIN model checker

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- Bounds data races in *space* and *time*
  - ★ Data races on one location do not affect sequential semantics of another
  - ★ Dara races in the past or the future do no affect sequential semantics of non-racy accesses

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- Must preserve load-store ordering
  - ★ Most compiler optimisations are valid (CSE, LICM).
    - ✦ No redundant store elimination across load.
  - ★ Free on x86, low-overhead on ARM (0.6% overhead) and POWER (2.9% overhead)

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- WIP to support capturing continuations that include C frames c.f "Threads Yield Continuations"

Status

- Major GC and fiber implementations are stable modulo bugs
  - ★ *TODO: Effect System*
- Laundry list of minor features
  - ★ https://github.com/ocamllabs/ocaml-multicore/projects/3
- We need
  - ★ Benchmarks
  - ★ Benchmarking tools and infrastructure
  - ★ Performance tuning

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- Verify multicore OCaml programs
  - ★ Explore (semi-)automated SMT-aided verification
  - ★ Challenge problem: verify k-CAS at the heart of Reagents library

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- Multicore-capable *Irmin*, a branch-consistent database library

Future Directions: Heterogeneous System

- Programming heterogenous, non Von Neumann architectures
  - ★ How do we capture computational model in richer type system?
  - ★ How do we compile efficiently to such a system?