Functional Abstractions for Practical and Scalable Concurrent Programming

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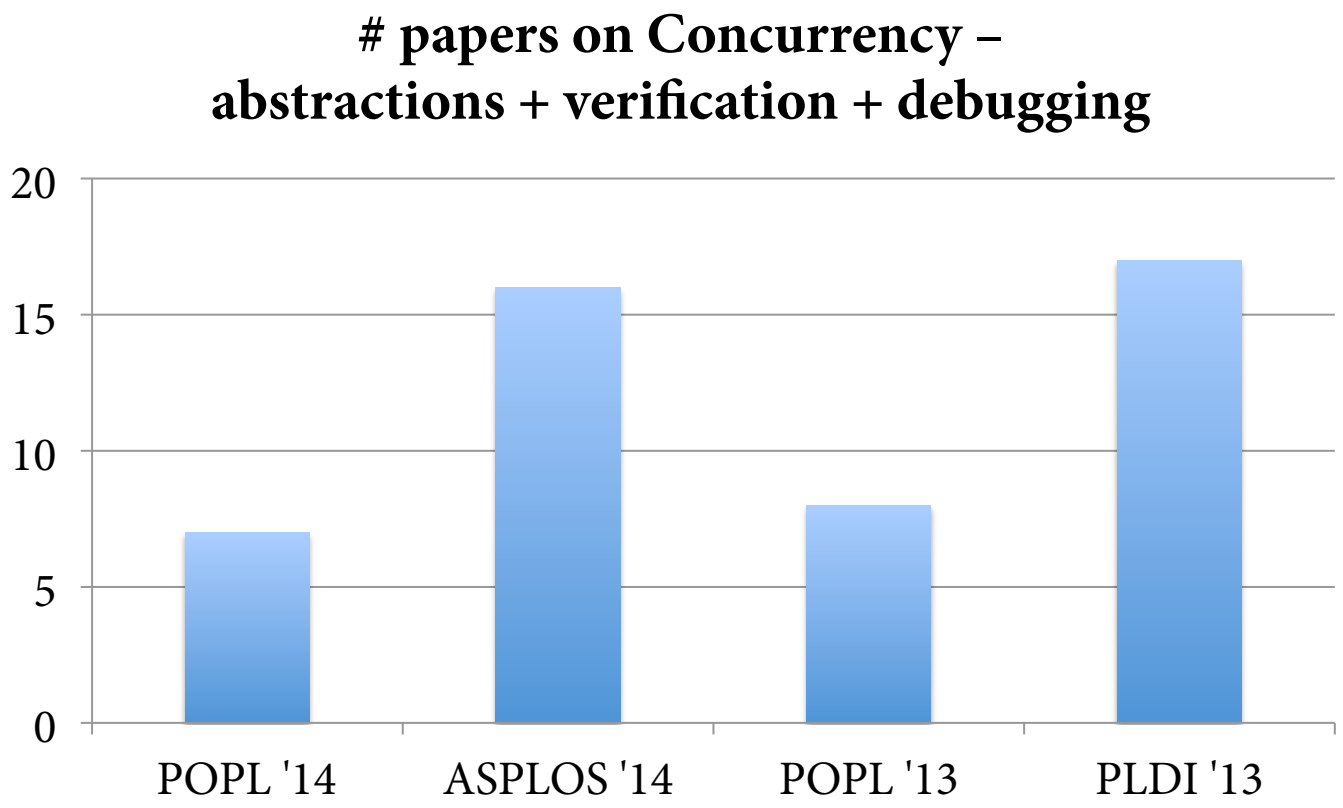
Purdue University

Concurrent programming is (still) hard!



Concurrency bugs can be disastrous

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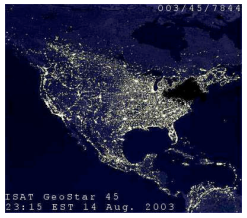
2003 Northeast blackout[1]



- Data race disables alarm system
- Effect
  - 256 power stations go offline
  - ~7 hr major blackout
  - 11 fatalities, $6 billion

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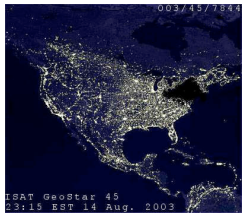

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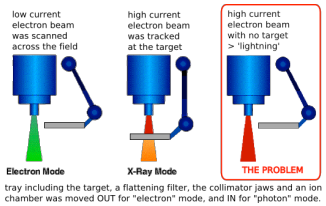
Therac-25 incidents[2]



- Data race b/w UI and controller
- 6 fatalities

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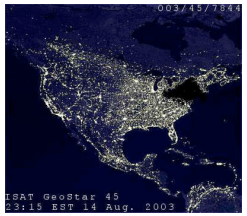

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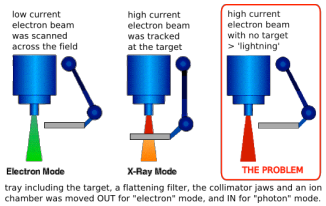

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Facebook IPO @ NASDAQ[3]

- Race between validation and new orders arrival
- NASDAQ compensation = $62 million

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Safe and scalable
concurrent program

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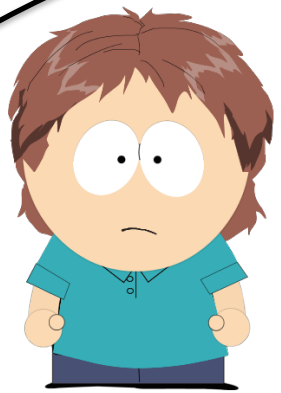
Fences, Locks,
Condition variables, etc.



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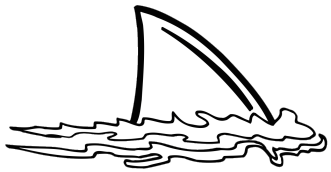
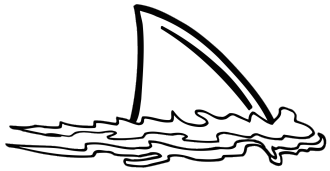


Data race



Deadlock

Fences, Locks,
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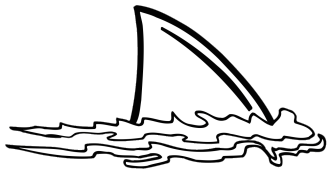
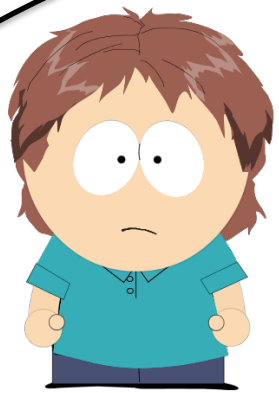


Atomicity
violations



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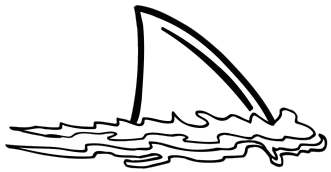

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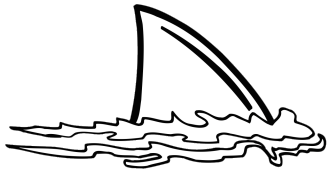
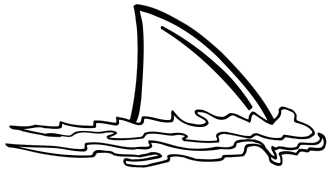


Weak memory
semantics



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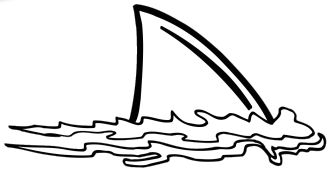
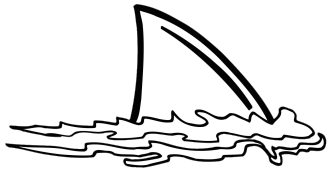
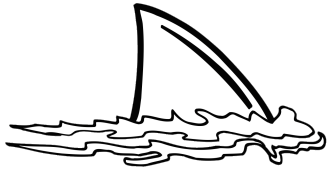


Eventual
consistency



No cache
coherence



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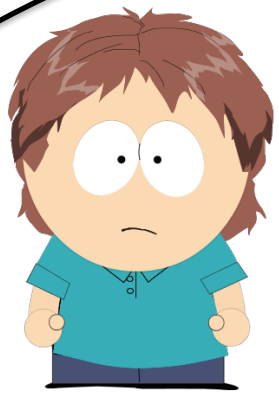

Stick to
Status Quo

Safe and scalable
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Testing

Safe and scalable concurrent program

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Testing

Verification

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PL Support

Safe and scalable concurrent program

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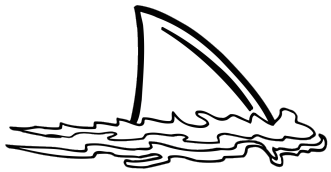
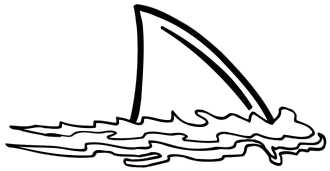


Data race



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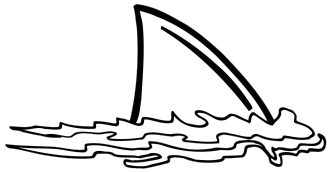
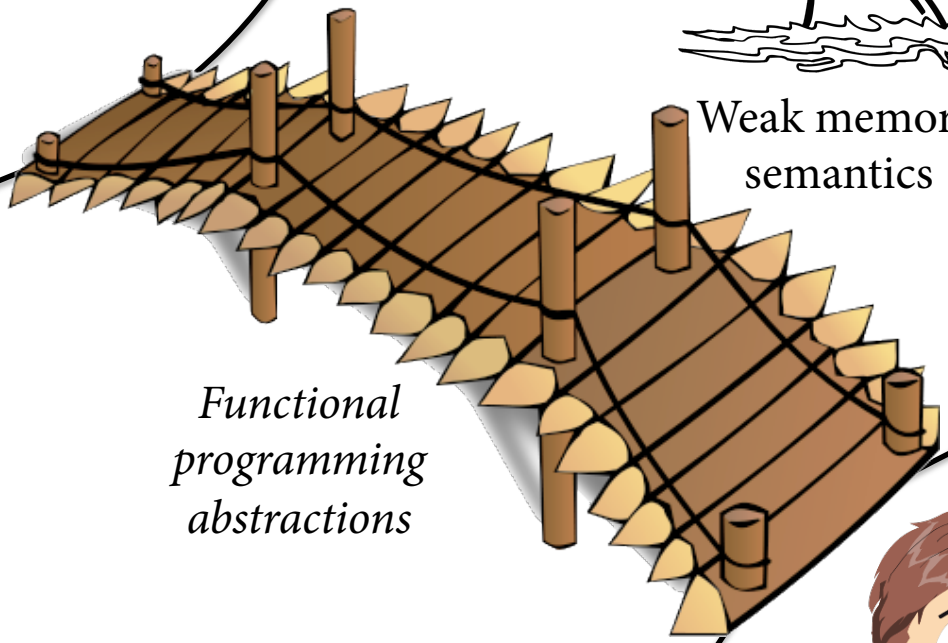
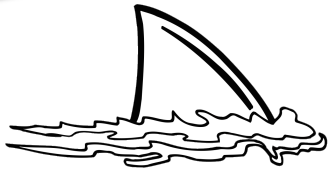


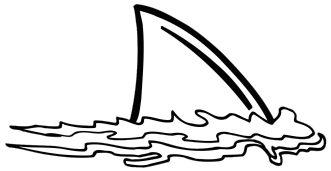
Weak memory semantics



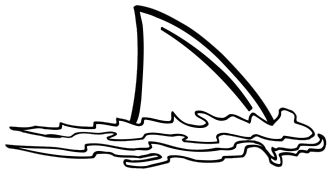
Functional programming abstractions



Eventual consistency



Non-cache coherence



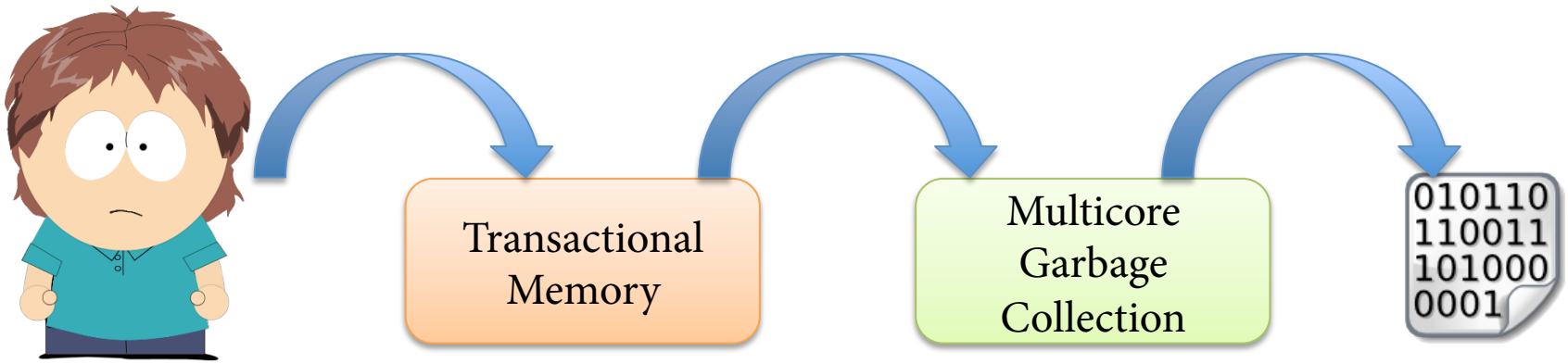
Atomicity violations

Programming abstractions *simplify* Concurrent Programming

Transactional Memory

Multicore Garbage Collection

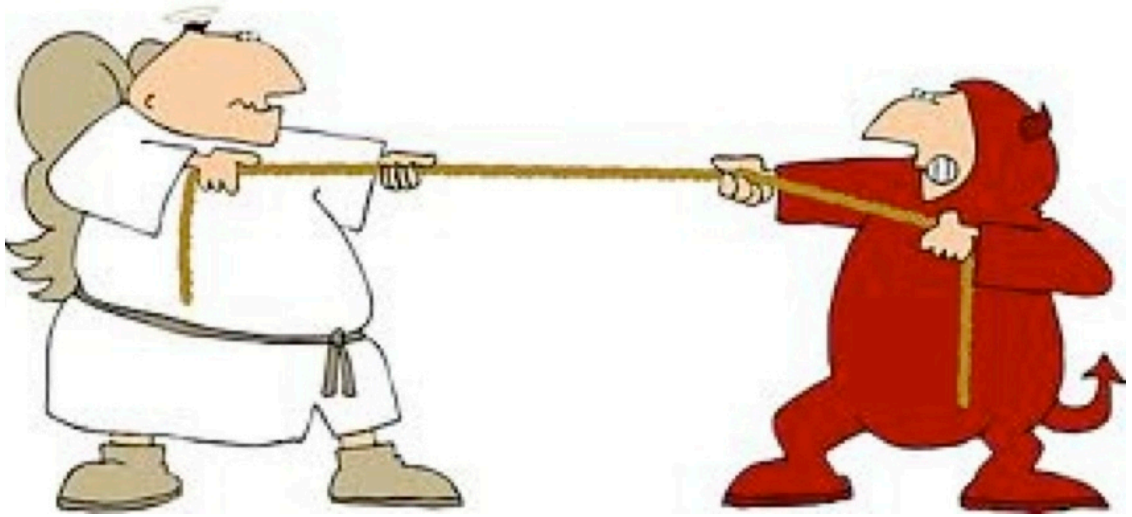
But, programming abstractions introduce a *level of indirection*



Slower than locks under high contention

Stop-the-world GC hinders scalability

Safety
&
Simplicity



Performance
&
Functionality

Safety
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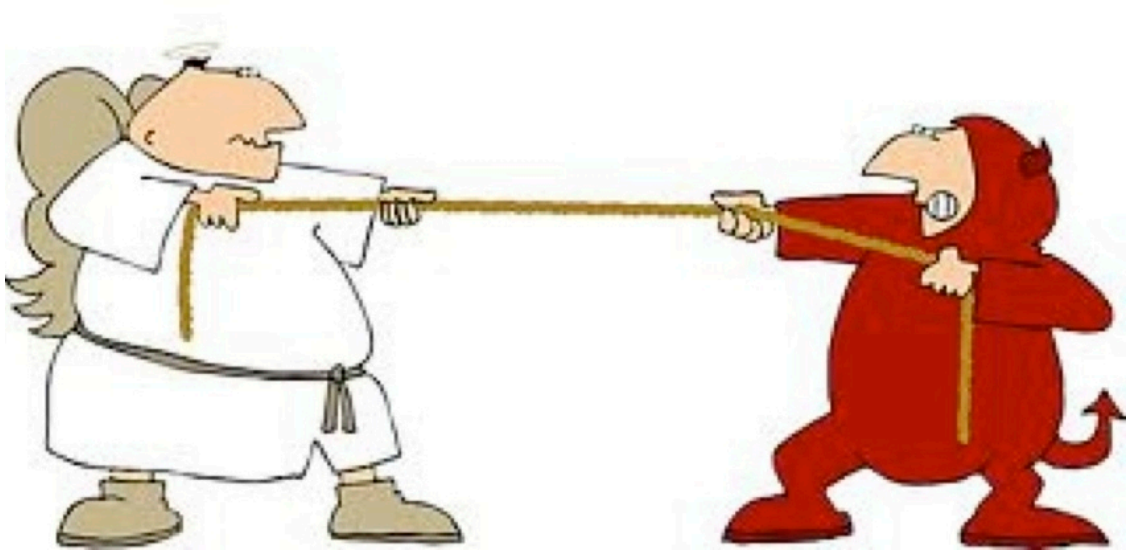
Simplicity



Performance
&
Functionality

Always desirable to marry the two whenever possible!

MultiMLton

Intel SCC
48-core Non-cache-coherent

Azul Vega 3
864-core CC-UMA

Compute clouds

Windows Azure

amazon web services™

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Language Design

Asynchronous CML [PLDI '11]
Memoizing Communication [ICFP '09]
Rx-CML – optimistic CML [PADL '14]

Runtime Systems

Parasitic threads [DAMP '10, JFP '14]
Thread-local GC [ISMM '12, MARC '12, JFP '14]

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Scheduler activations for Haskell

Schedulers for Haskell threads as Haskell libraries
[In submission to OOPSLA '14]

Sting (Java)

Session type based protocol optimization
[Coordination '10, SCP '13]

MultiMLton

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Rx-CML : A Prescription for Safely Relaxing Synchrony

Abstraction	Synchronous communication	Transactional memory	Garbage collection
			
Domain	Asynchronous distributed system	Shared memory concurrency	Memory management

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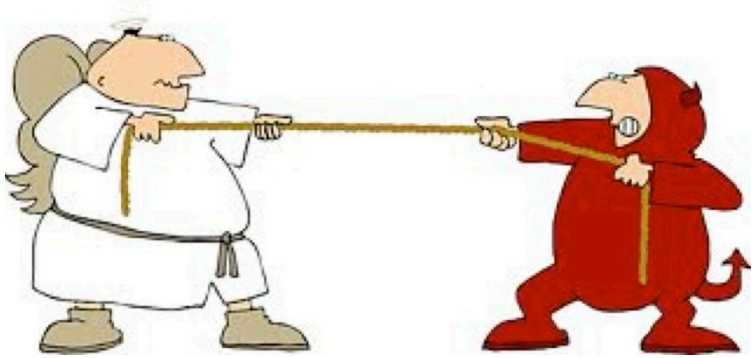

synchrony latency

Can we discharge synchronous communications asynchronously and ensure observable equivalence?

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Formalize:

$$[\![\, \texttt{send}\,(c, v)]\!]k \;\equiv\; [\![\, \texttt{asend}\,(c, v)]\!]k$$

Implement:

Distributed Concurrent ML in MultiMLton +
Speculative execution framework

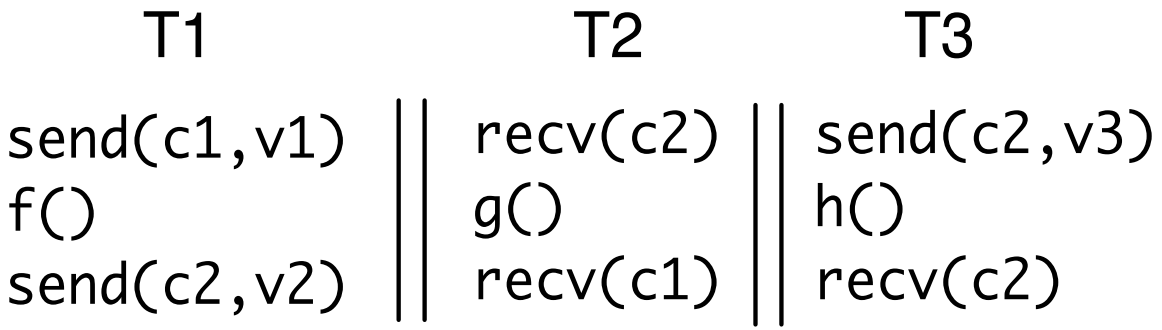
Concurrent ML

```
val spawn      : (unit -> unit) -> thread_id

val channel    : unit -> 'a chan
val send       : 'a chan * 'a -> unit
val recv       : 'a chan -> 'a

val sendEvt    : 'a chan * 'a -> unit event
val recvEvt    : 'a chan -> 'a event
val sync       : 'a event -> 'a
val never      : 'a event
val alwaysEvt  : 'a -> 'a event
val wrap       : 'a event -> ('a -> 'b) -> 'b event
val guard      : (unit -> 'a event) -> 'a event
val choose     : 'a event list -> 'a event
...
```

Thread creation

Synchronous message passing

First-class events


T1
T2
T3
send(c1,v1)
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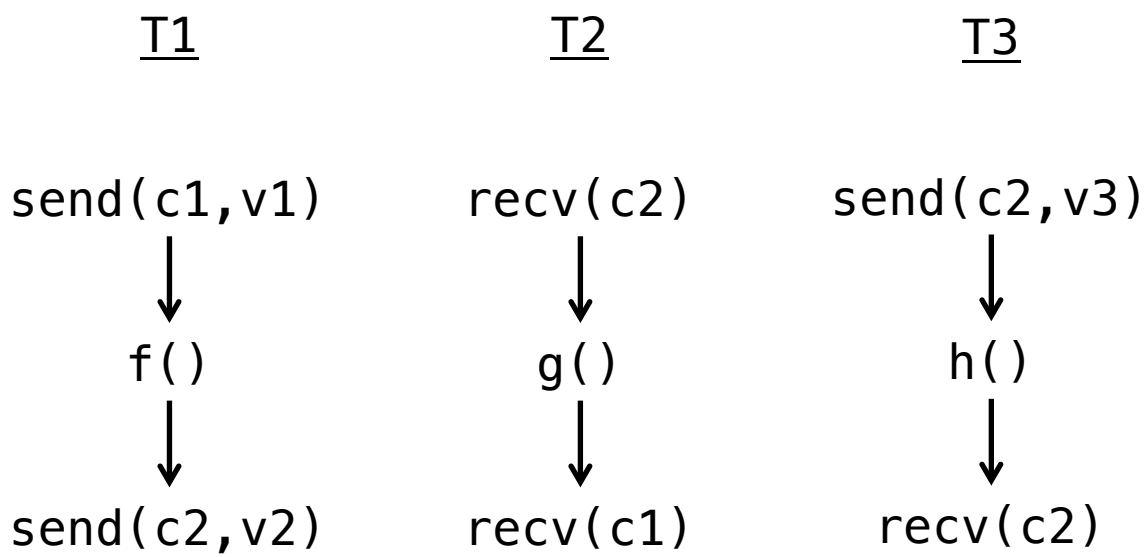
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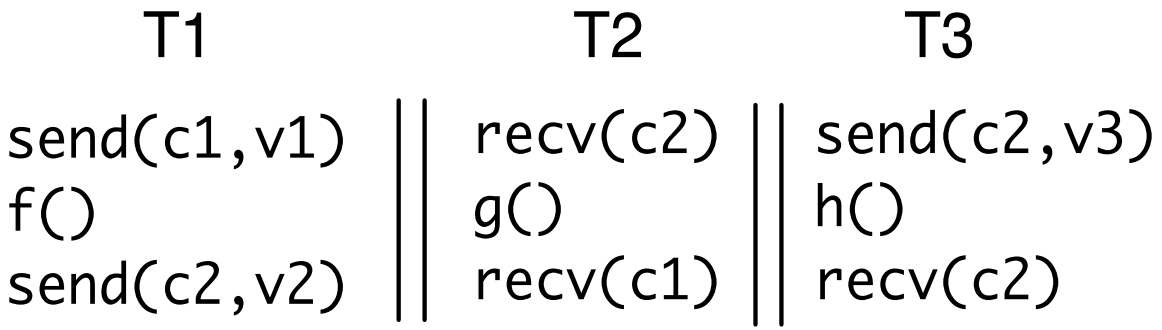
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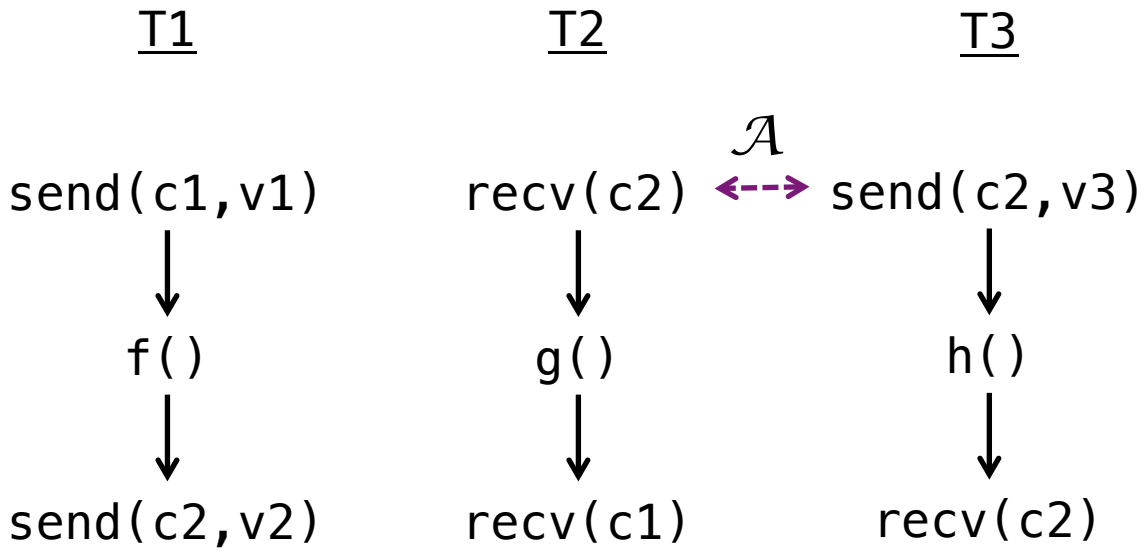
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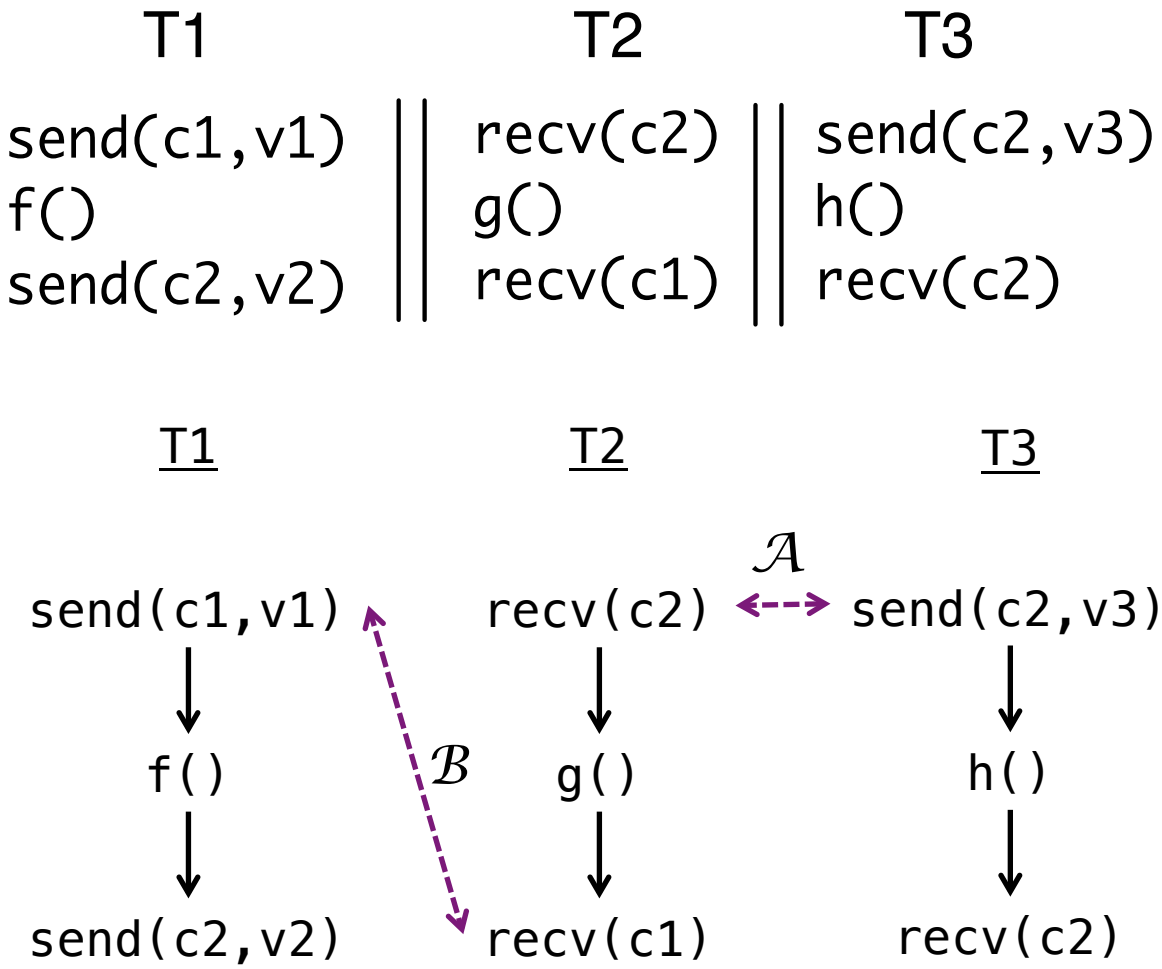
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A
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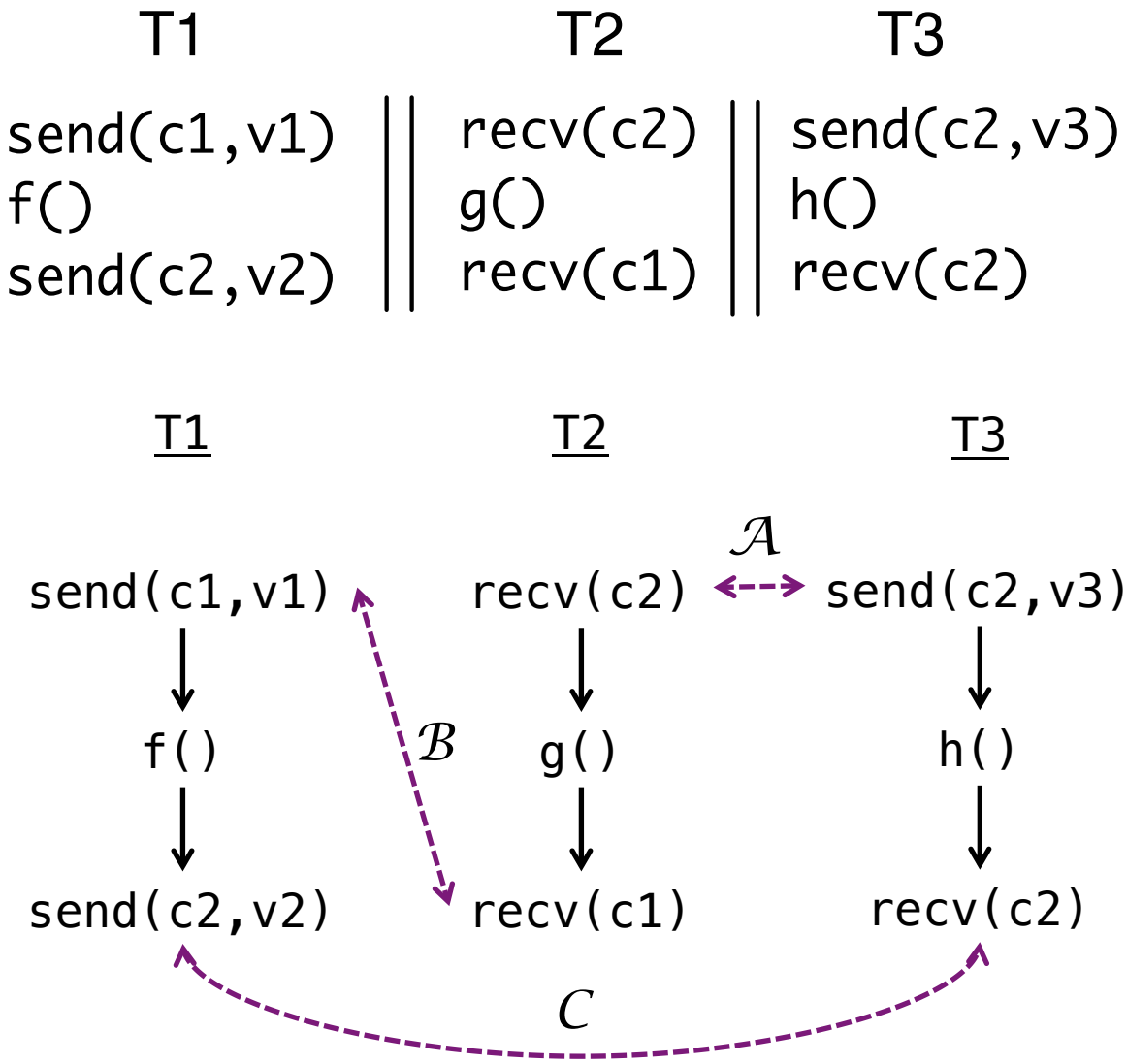
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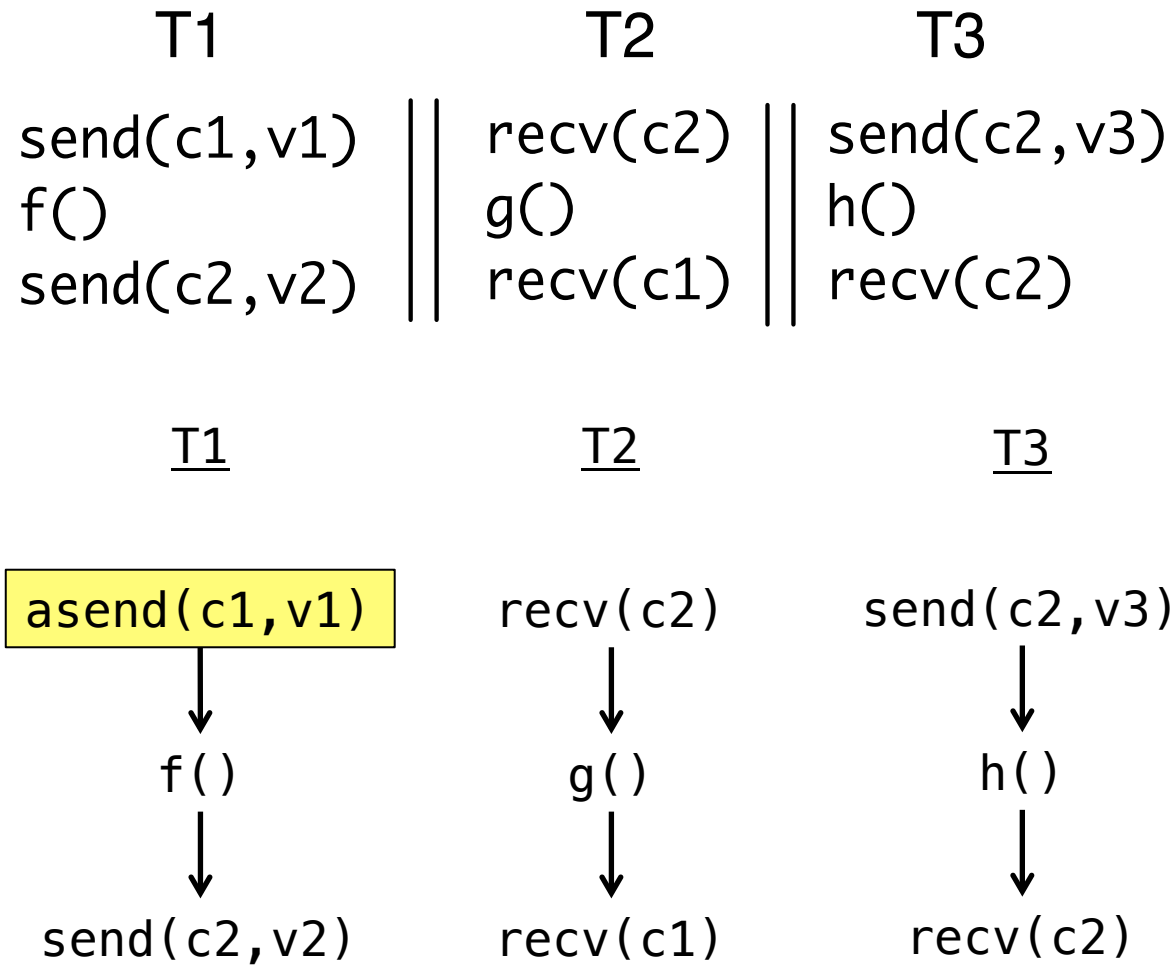
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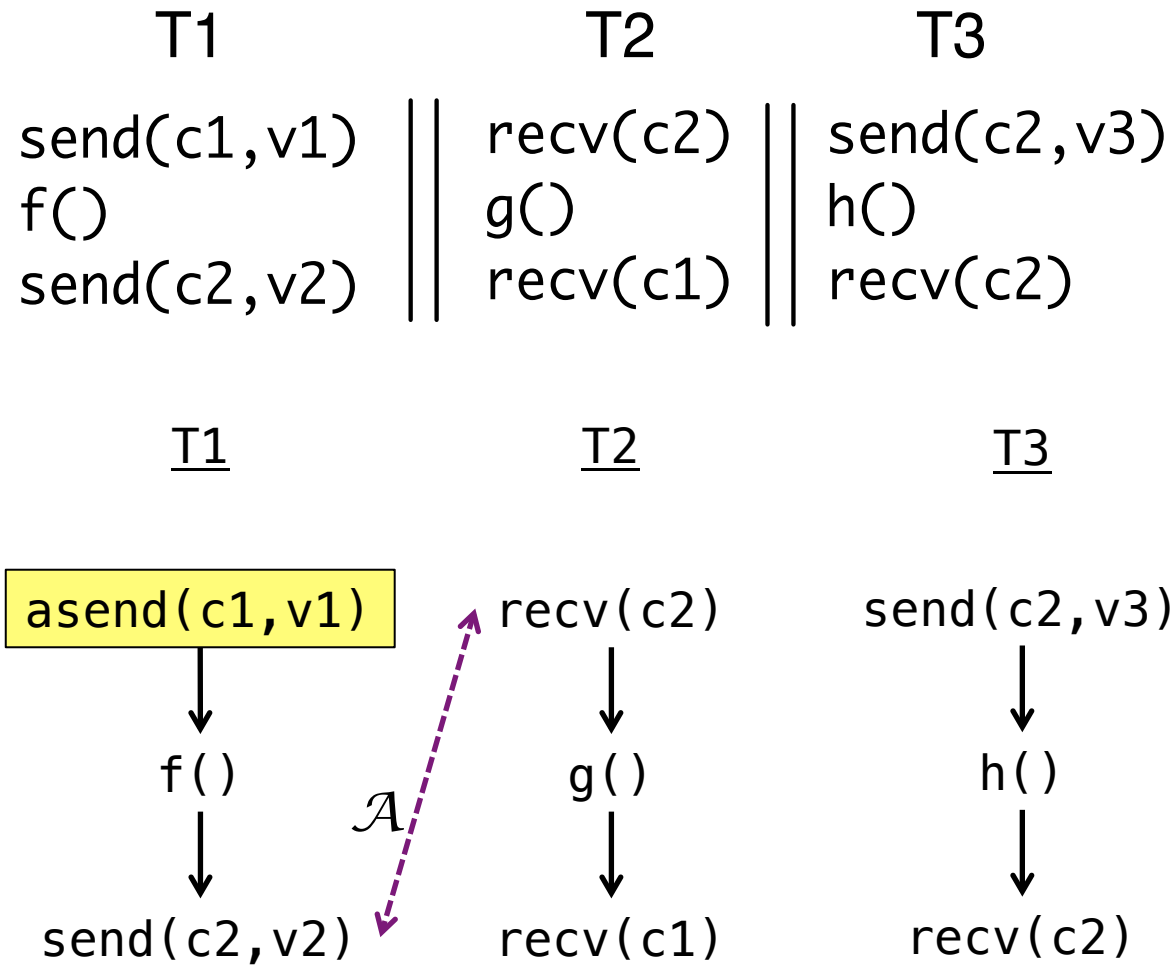
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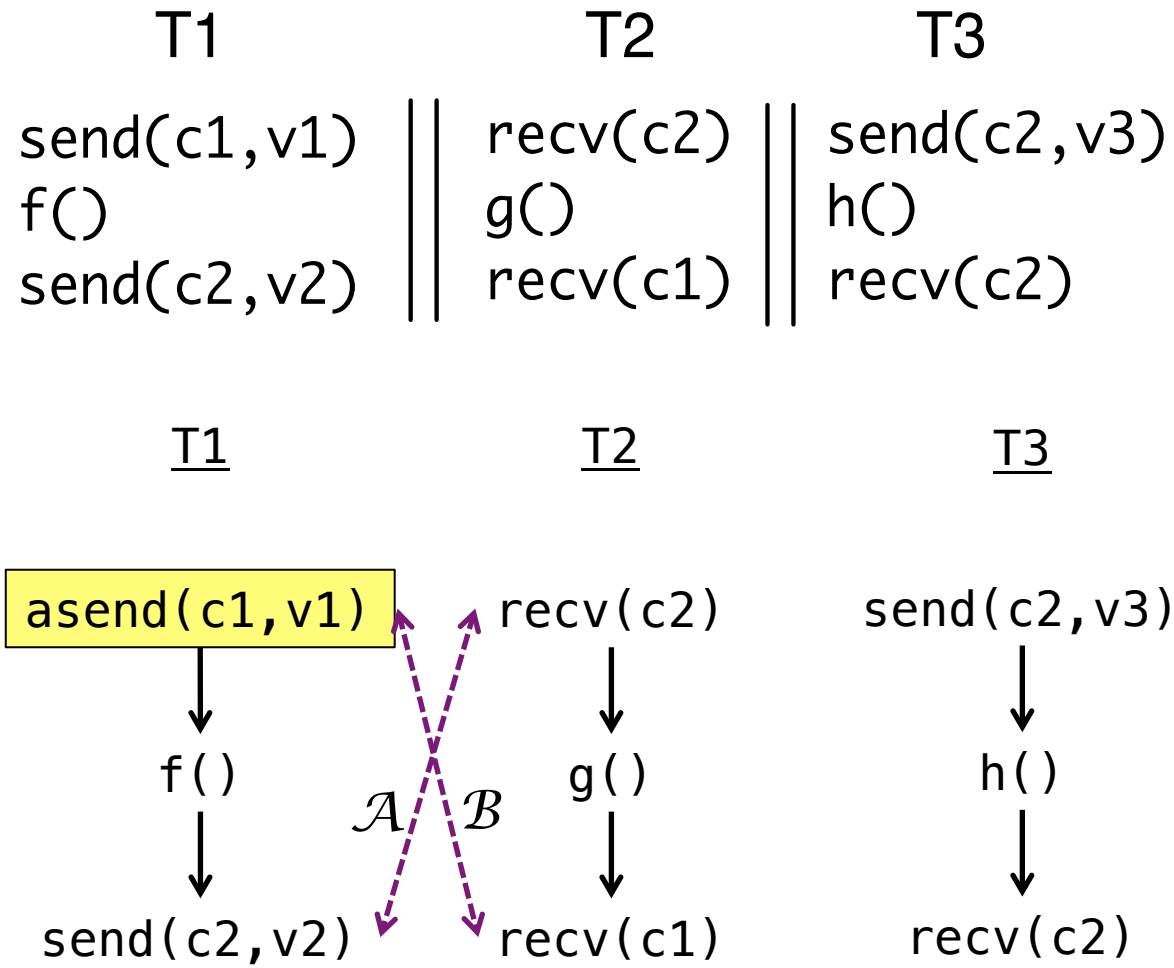
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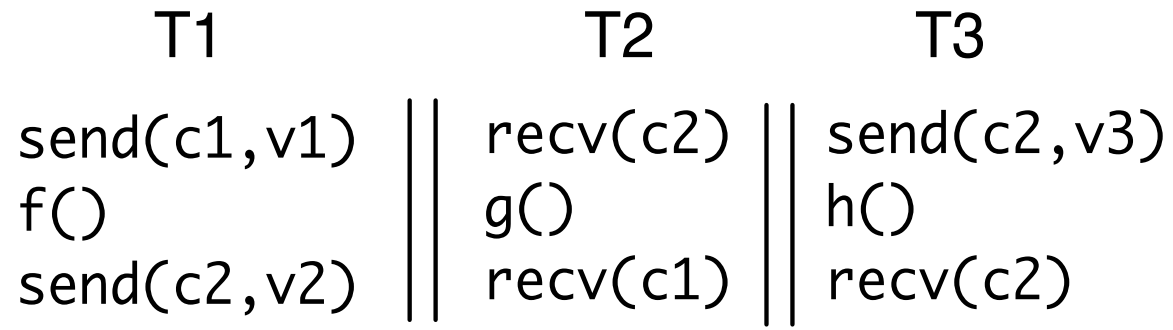
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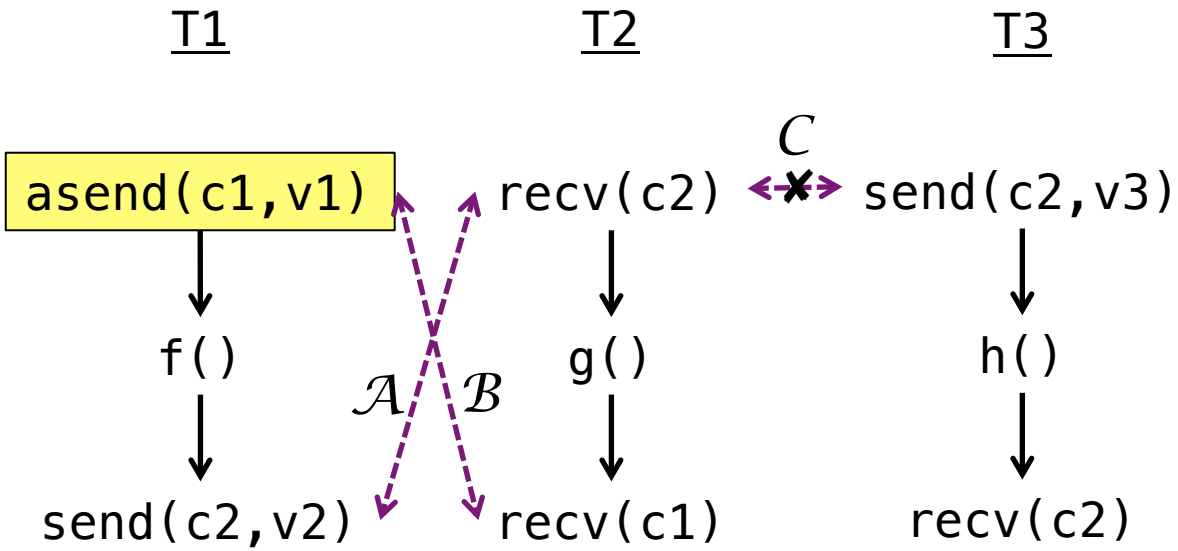
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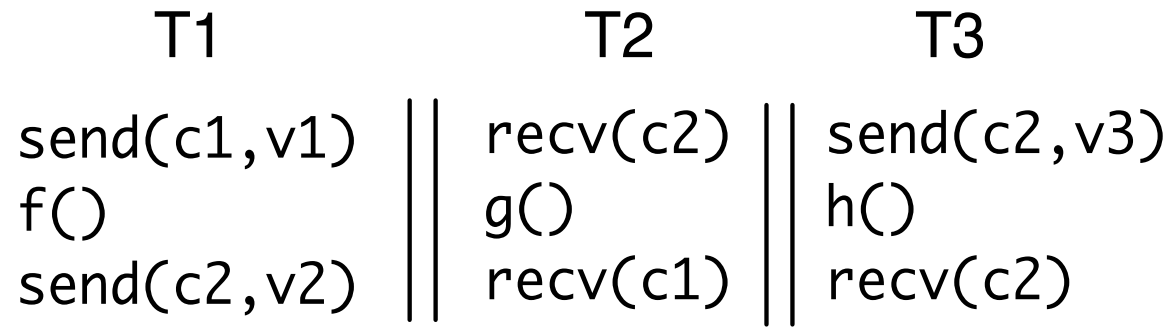
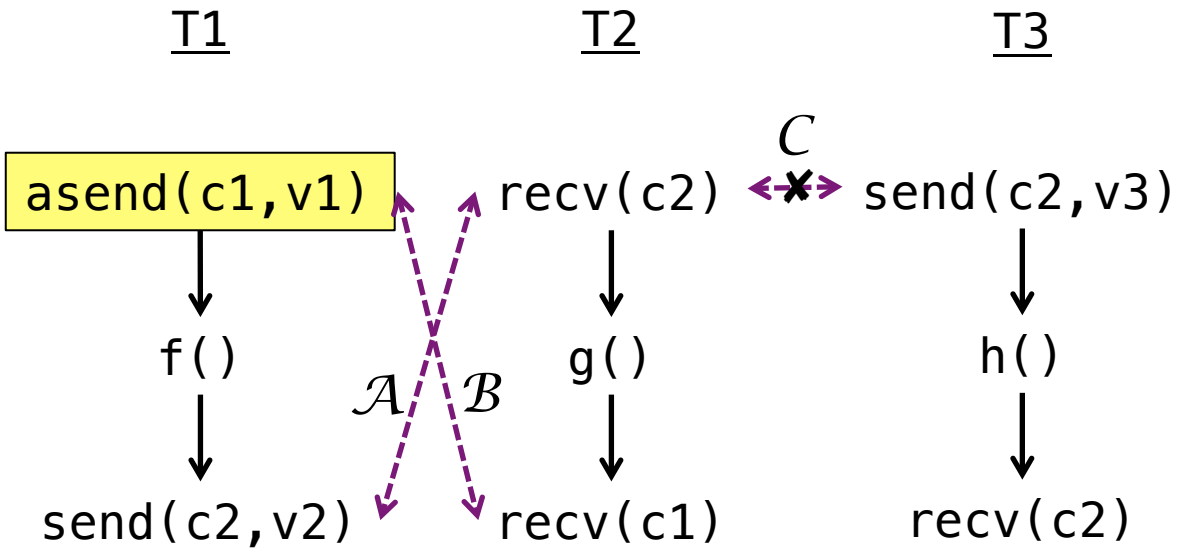
recv(c2)
send(c2,v3)
f()
g()
h()
A
B
send(c2,v2)
recv(c1)
recv(c2)





Cyclic dependence ⇒ divergent behavior

Distributed group chat app

No central server & causal dependence → *causal broadcast*

Distributed group chat app

No central server & causal dependence → *causal broadcast*

```
fun bsend (BCHAN (vcList, acList), v: 'a, id: int) : unit =
let
  val _ = map (fn vc => if (vc = nth (vcList, id)) then () else send (vc, v))
              vcList (* phase 1 -- Value distribution *)
  val _ = map (fn ac => if (ac = nth (acList, id)) then () else recv ac)
              acList (* phase 2 -- Acknowledgments *)
in ()
end
```

synchronously send values

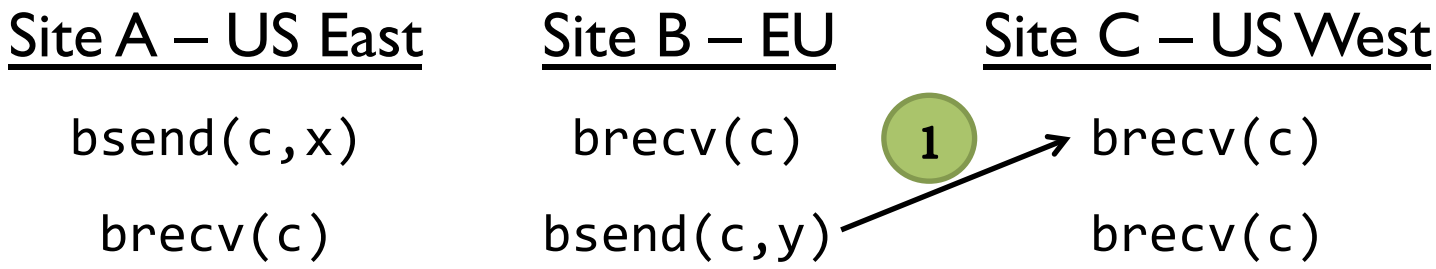
prevent receivers from proceeding until all members have received the value

Distributed group chat app: Performance

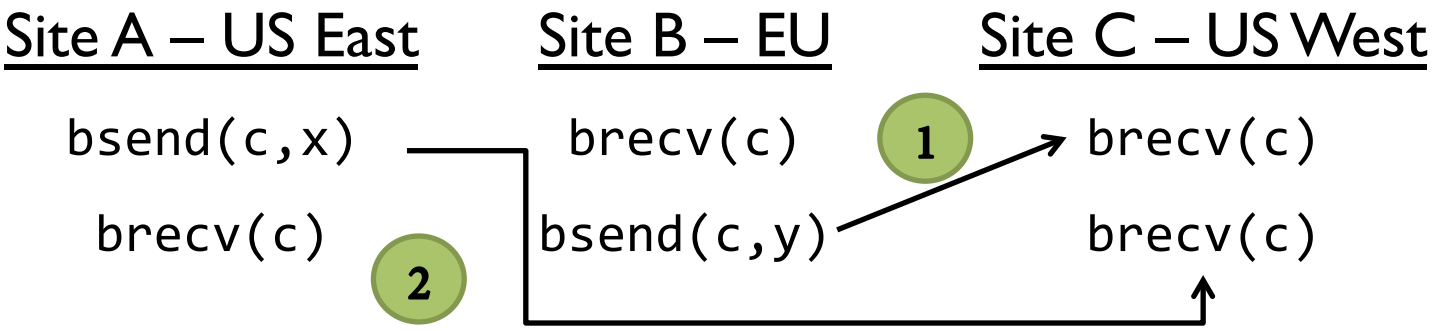
Distributed group chat app: Performance

Site A – US East	Site B – EU	Site C – US West
`bsend(c,x)`	`brecv(c)`	`brecv(c)`
`brecv(c)`	`bsend(c,y)`	`brecv(c)`

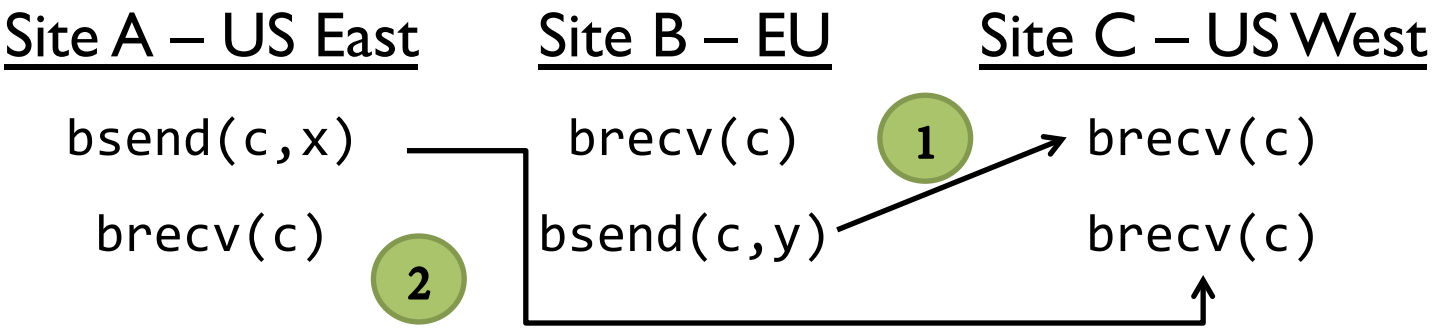
Distributed group chat app: Performance



Distributed group chat app: Performance



Distributed group chat app: Performance



Execution	*Avg.time (ms)*	*Errors*
Sync	1540	0
Unsafe Async	520	7
Safe Async ($\mathbb{R}^{\text{CML}}$)	533	0

Formalization

Reason axiomatically

$$\mathrm{E} := \langle \mathrm{P}, \mathrm{A}, \rightarrow_{po}, \rightarrow_{co} \rangle$$

Happens-before relation

$$\begin{aligned} \rightarrow_{hb} \quad = \quad & (\rightarrow_{po} \cup \rightarrow_{td} \cup \\ & \{(\alpha, \beta) \mid \alpha \rightarrow_{co} \alpha' \wedge \alpha' \rightarrow_{po} \beta\} \cup \\ & \{(\beta, \alpha) \mid \beta \rightarrow_{po} \alpha' \wedge \alpha' \rightarrow_{co} \alpha\})^{+} \end{aligned}$$

Well-formed execution

$$\text{Obs (WF\_Exec (P))} \in \{\text{Obs (Sync\_Exec (P))}\}$$

Formalization

Reason axiomatically $\mathrm{E} := \langle \mathrm{P}, \mathrm{A}, \rightarrow_{po}, \rightarrow_{co} \rangle$

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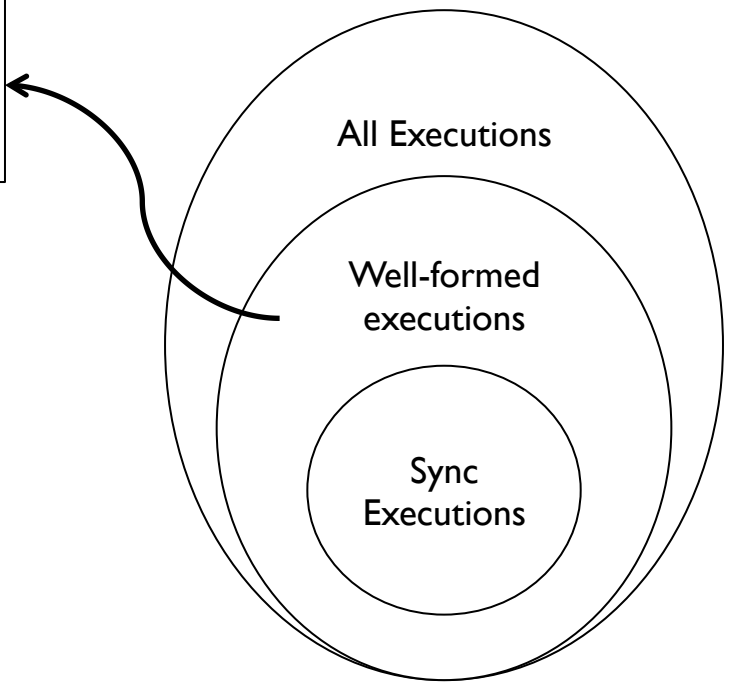
Well-formed execution $\text{Obs (WF\_Exec (P))} \in \{\text{Obs (Sync\_Exec (P))}\}$

- No happens before cycle
- Sensible intra-thread semantics
- No outstanding speculative actions



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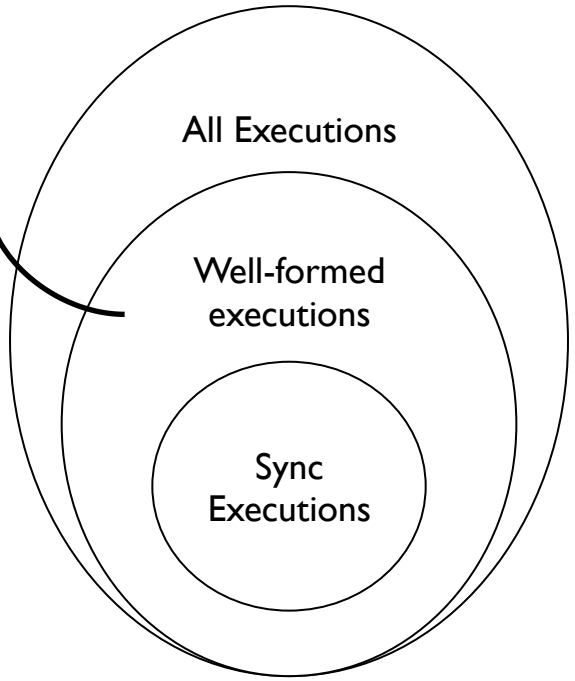
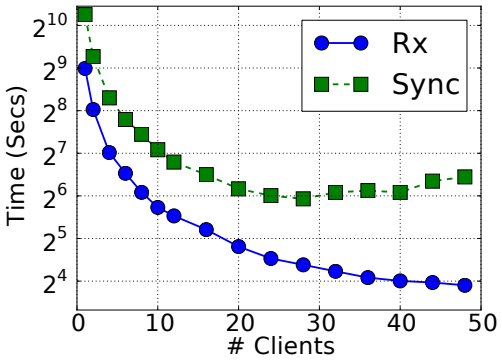
Recipe for implementation



Implementation & Results

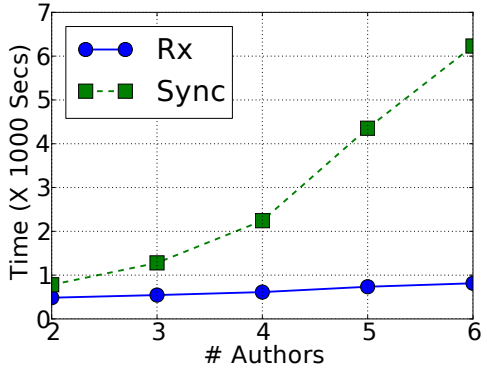
Implementation & Results

- Dependence graph ≡ Axiomatic execution
  - WF Check before observable actions
  - Ill-formed? Rollback and re-execute non-speculatively – Progress!
- WF Check, checkpoint, rollback are uncoordinated!
- Replicated channel consistency through speculative execution
- Benchmark: Optimistic OLTP & P2P Collaborative editing



OLTP

With 48 clients - 5.8X faster than sync
1.4X slower than async



Collaborative Editing

With 6 authors - 7.6X faster than sync
2.3X slower than async

Scheduler Activations in Haskell

How to write schedulers for Haskell threads as Haskell libraries?

How to write schedulers for Haskell threads as Haskell libraries in GHC?

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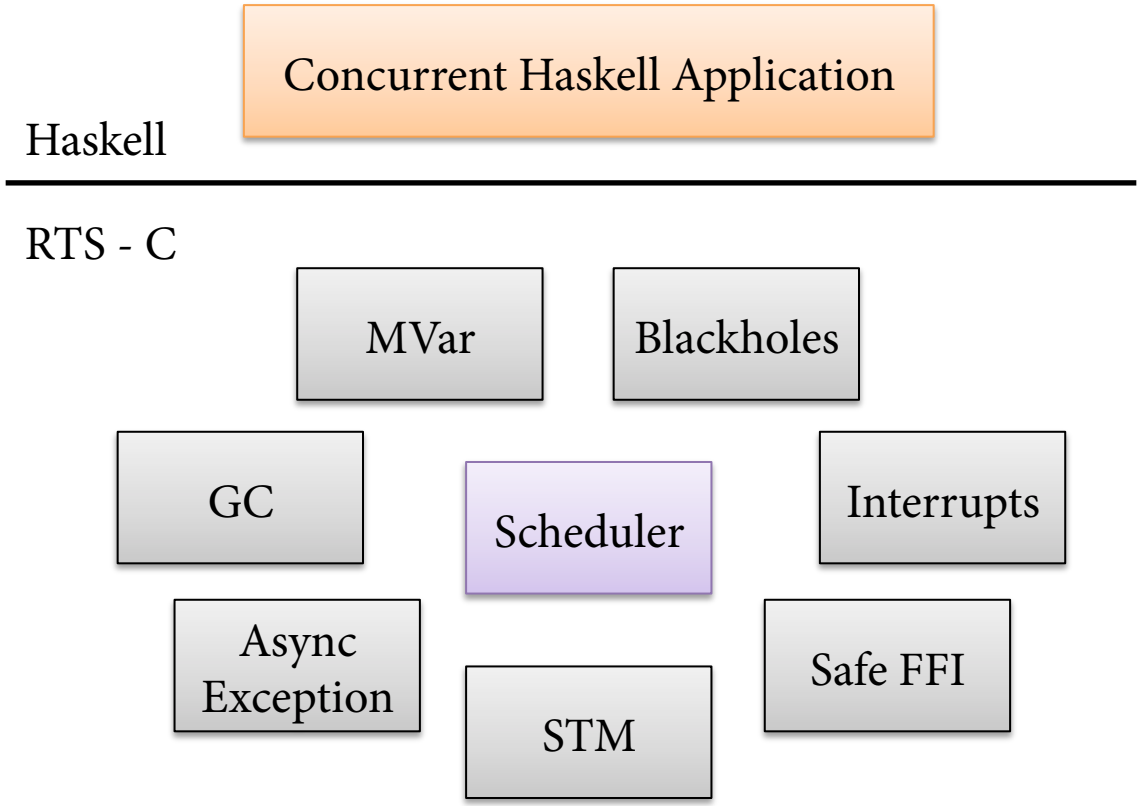

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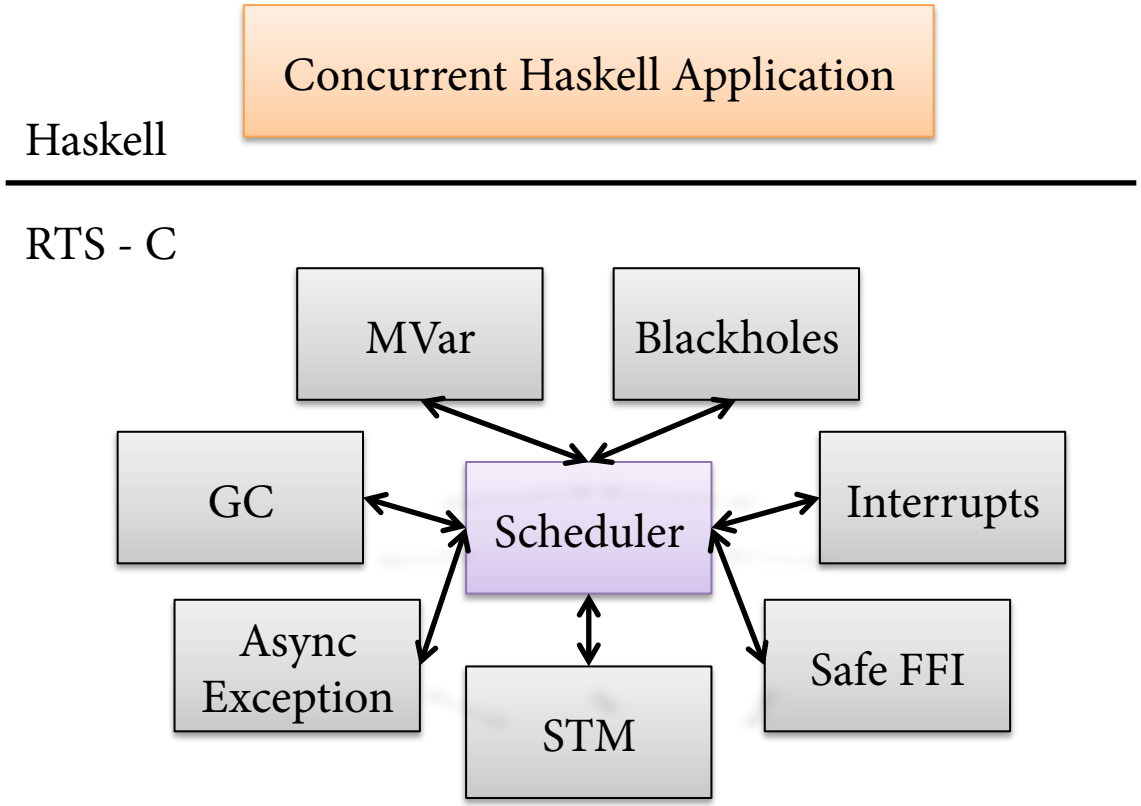

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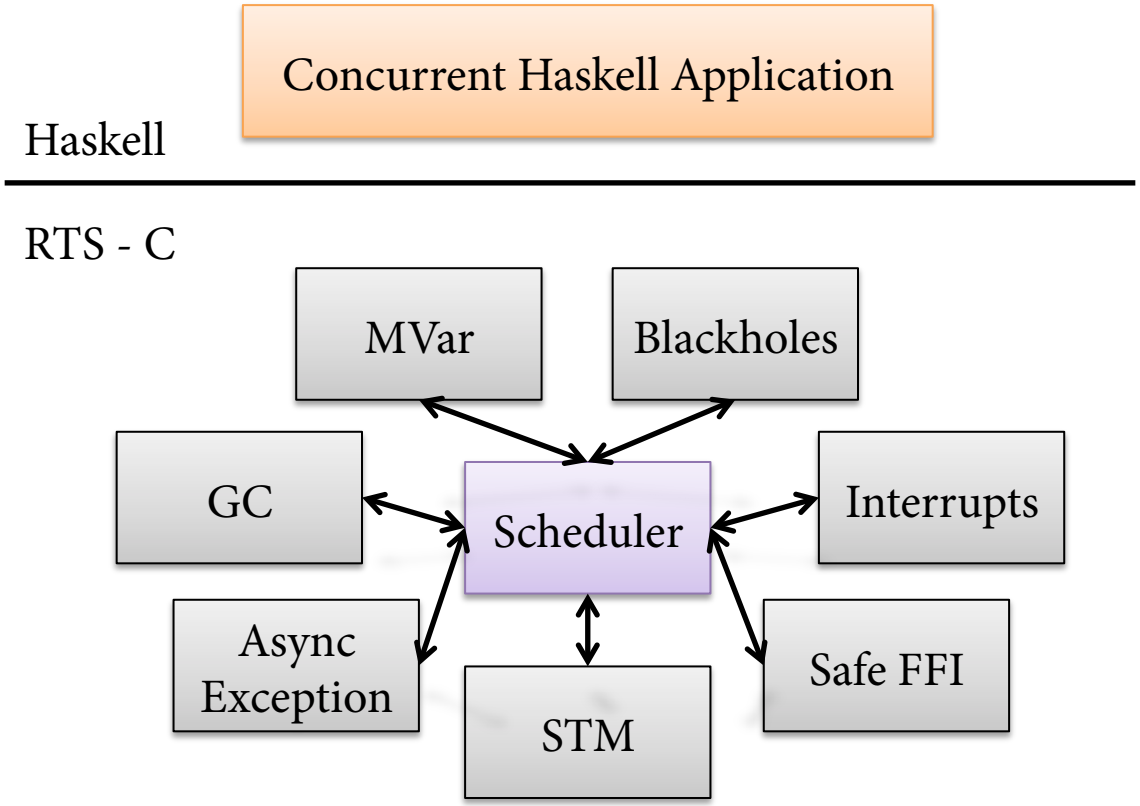
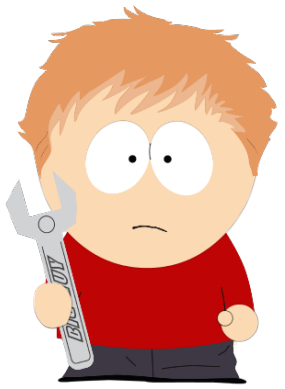
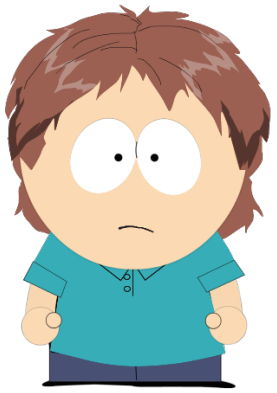


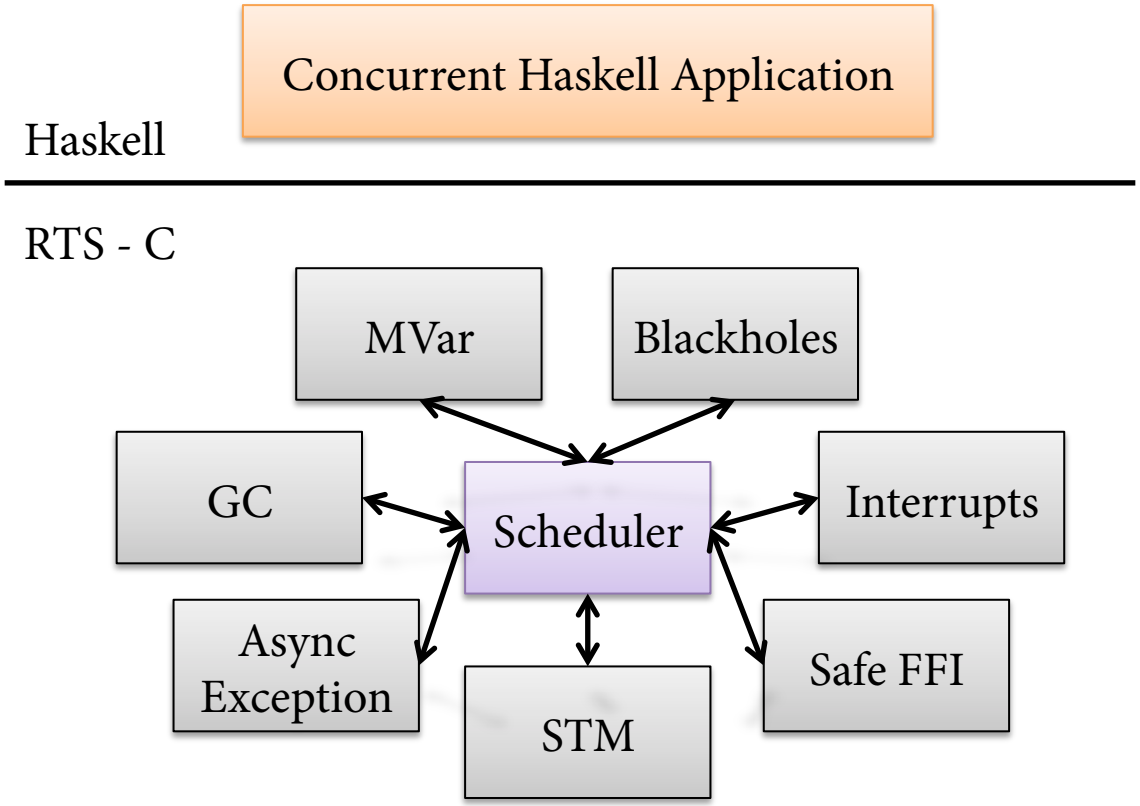


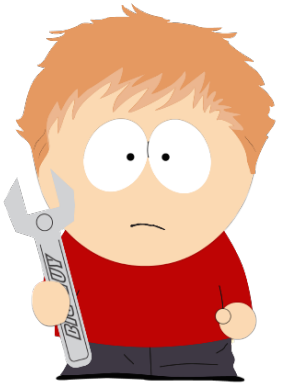
Lang Dev

How to write schedulers for Haskell threads as Haskell libraries in GHC?

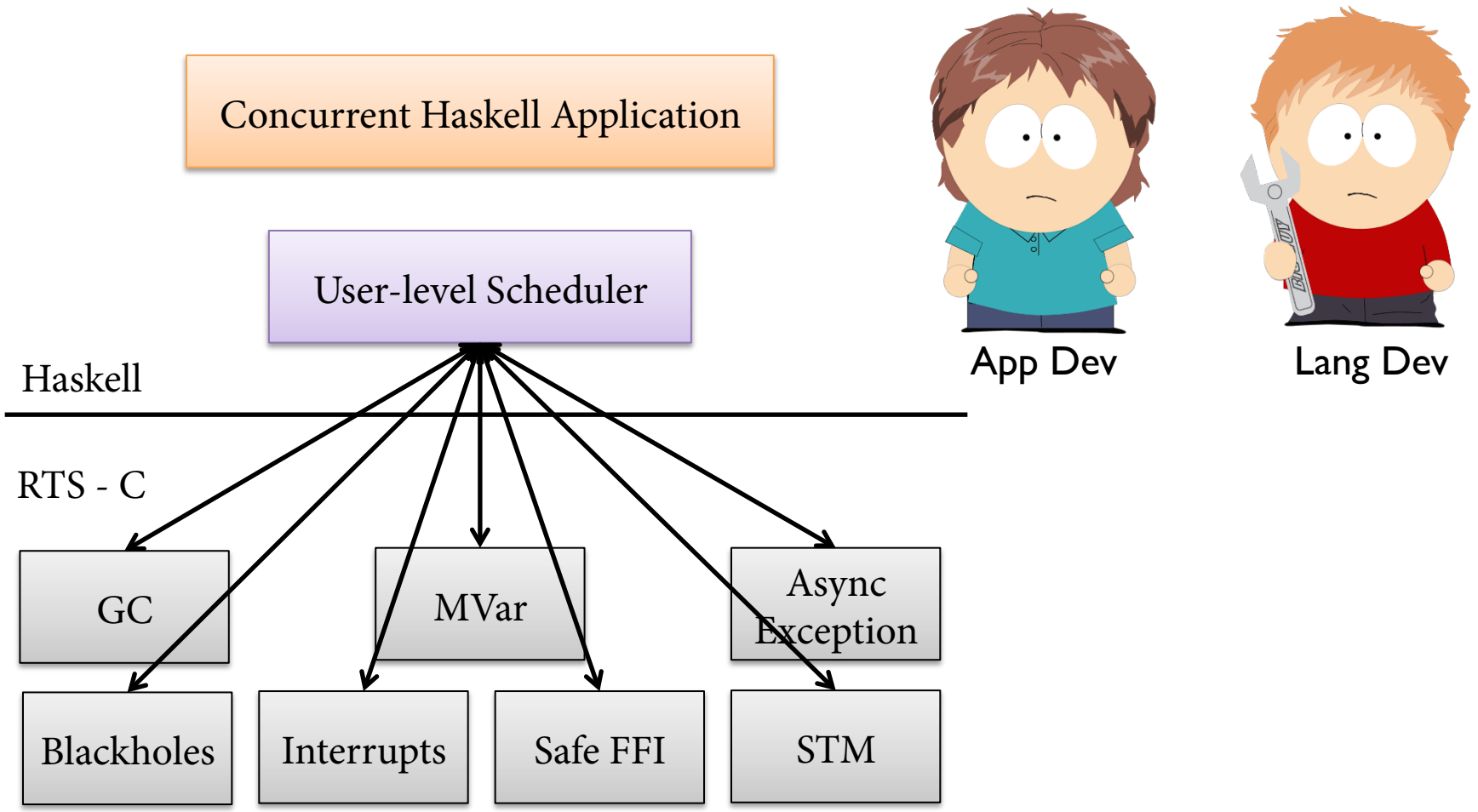


App Dev





Lang Dev


Concurrent Haskell Application
User-level Scheduler
Haskell
RTS - C
GC
MVar
Async Exception
Blackholes
Interrupts
Safe FFI
STM
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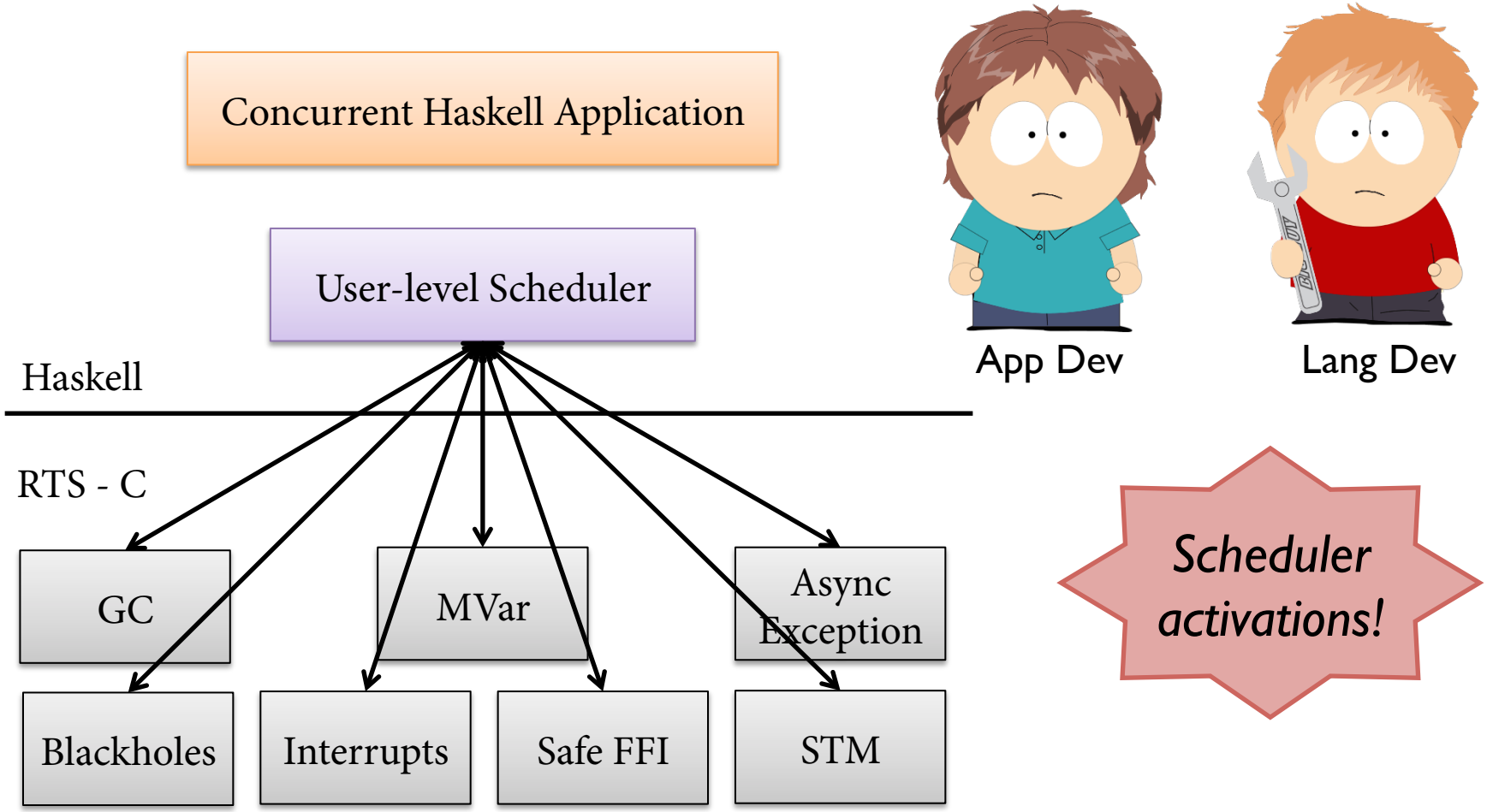
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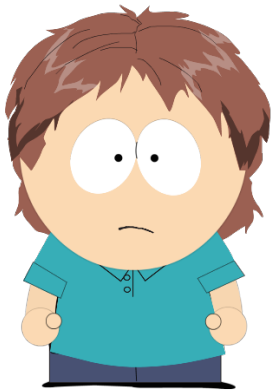
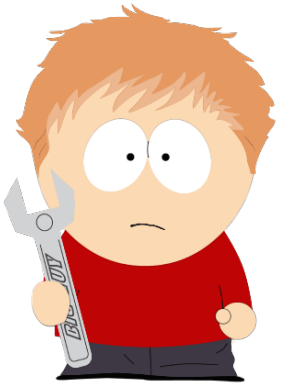
Scheduler activations!

Concurrent Haskell Application

User-level Scheduler



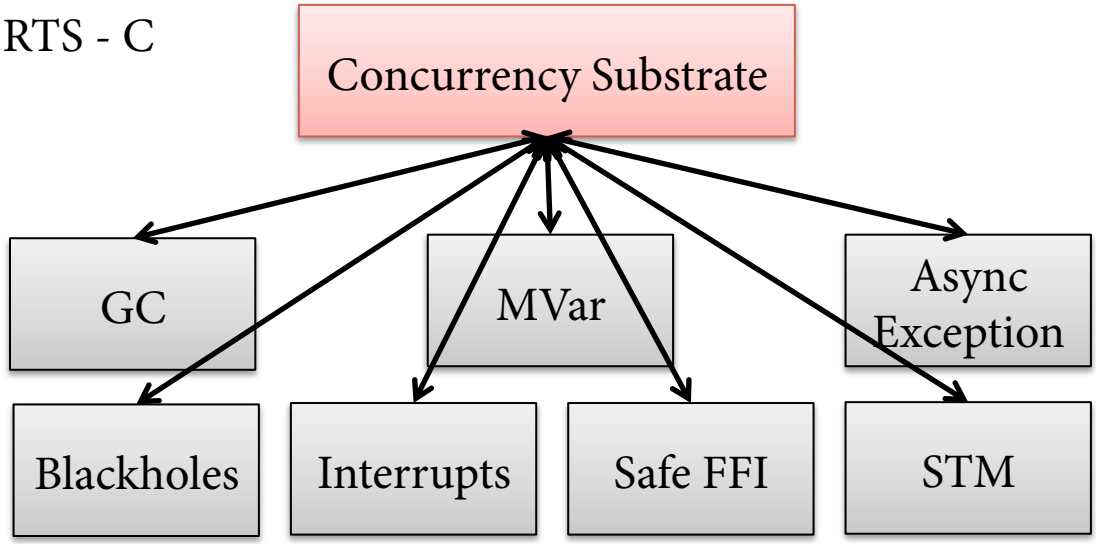
App Dev



Lang Dev

Haskell

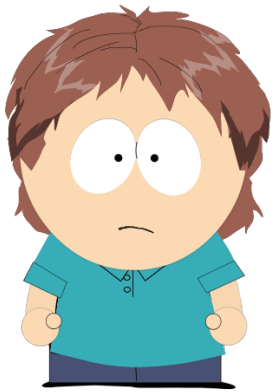
RTS - C



Concurrent Haskell Application

User-level Scheduler

EnQ and DeQ Activations



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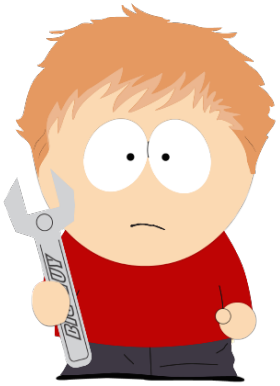

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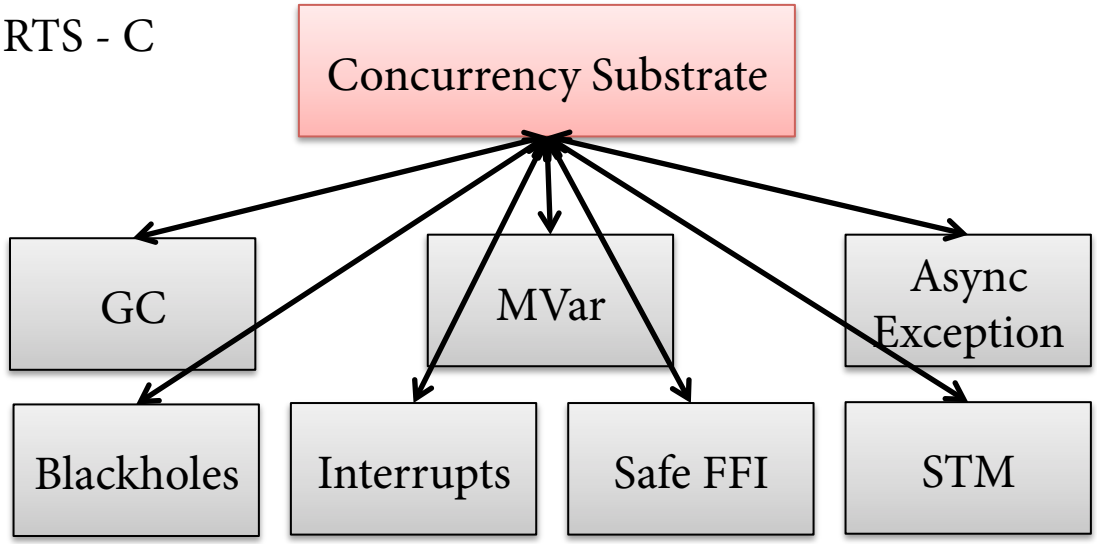

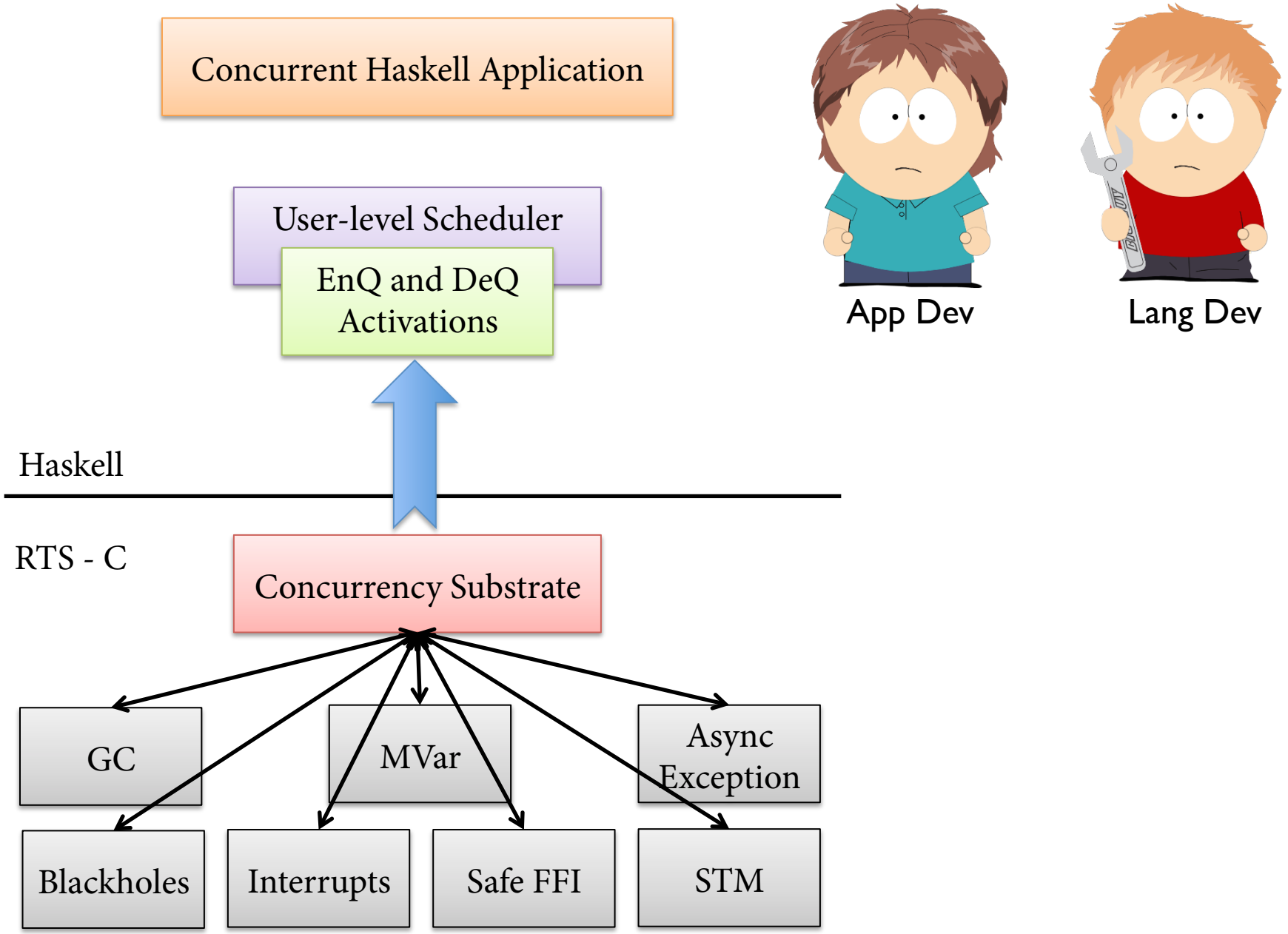
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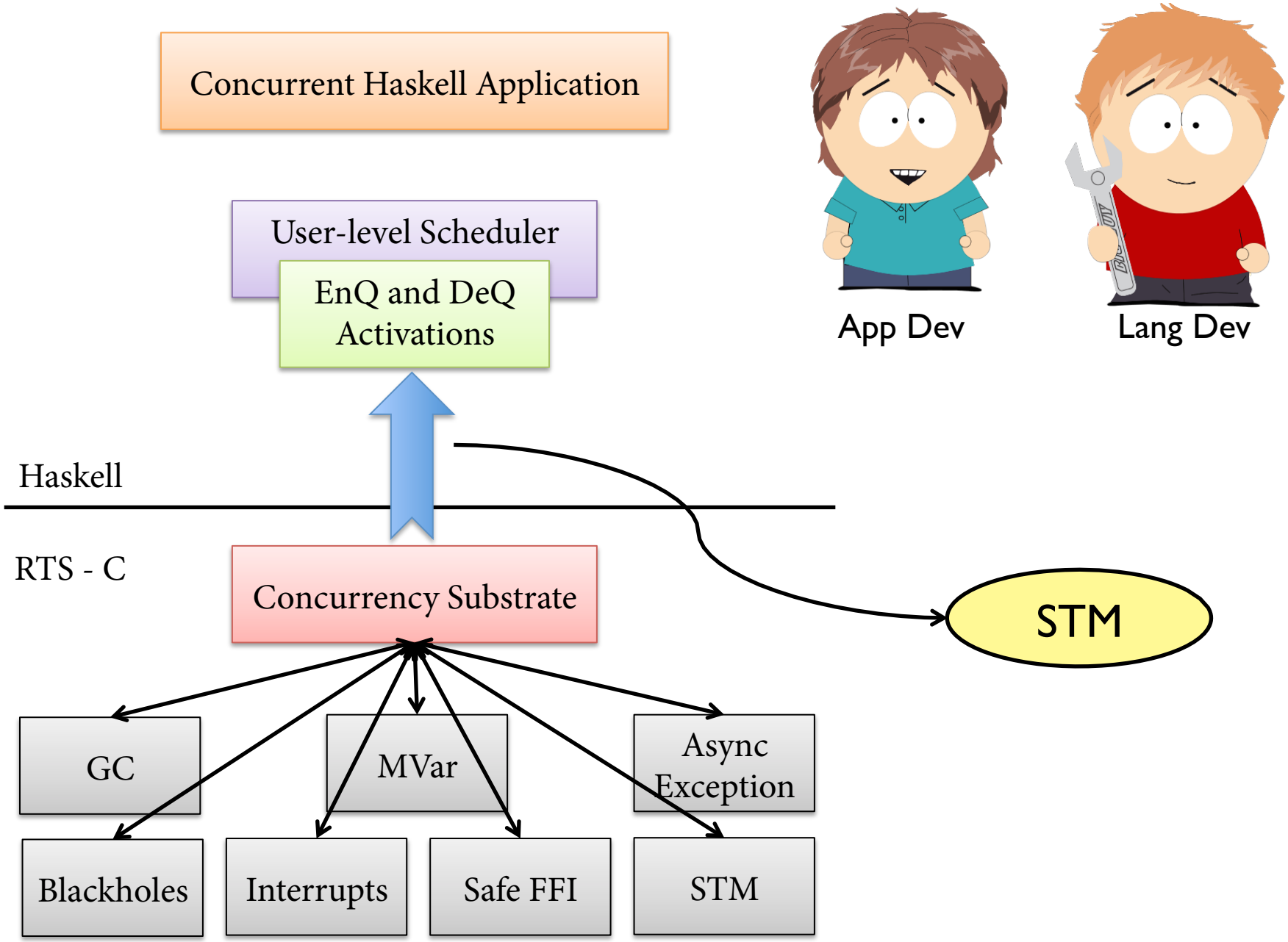
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Concurrency Substrate API

```
data SCont
newSCont      :: IO () -> IO SCont
switch        :: (SCont -> STM SCont) -> IO ()
runOnIdleHEC :: SCont -> IO ()
```

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-- read activations
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setDequeueAct  :: DequeueAct -> IO ()
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Scheduler access is under STM

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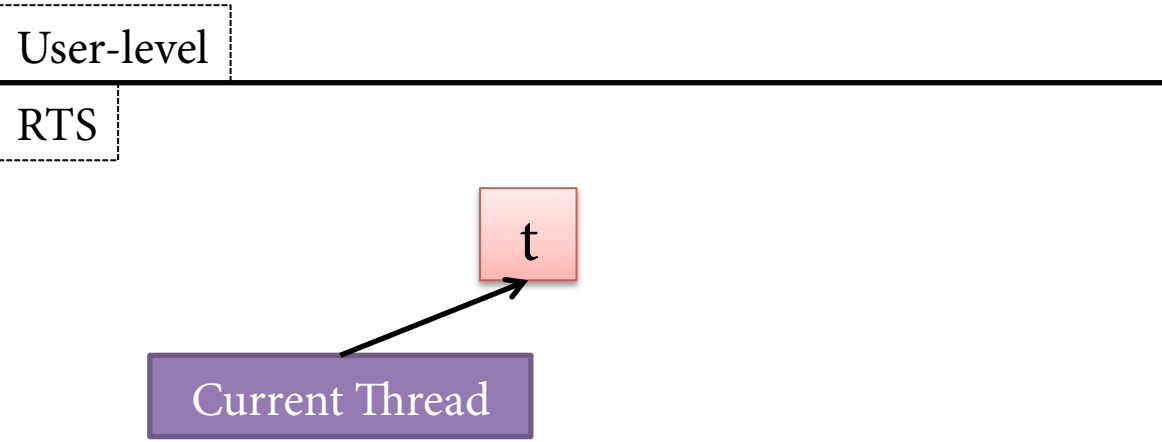
setDequeueAct  :: DequeueAct -> IO ()
setEnqueueAct  :: EnqueueAct -> IO ()

-- update activations
getAux         :: SCont -> STM Dynamic
setAux         :: SCont -> Dynamic -> STM ()
```

Scheduler access is under STM

RTS Interaction - Blocking



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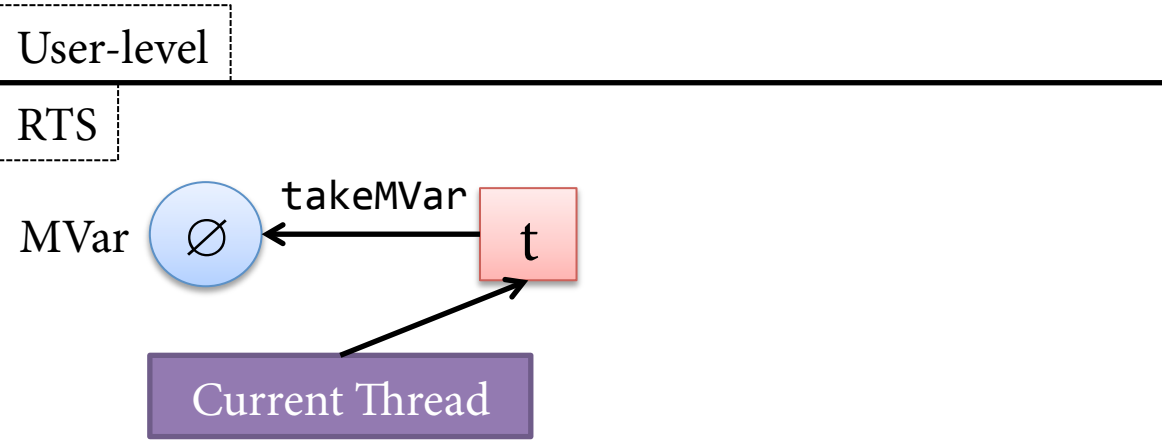

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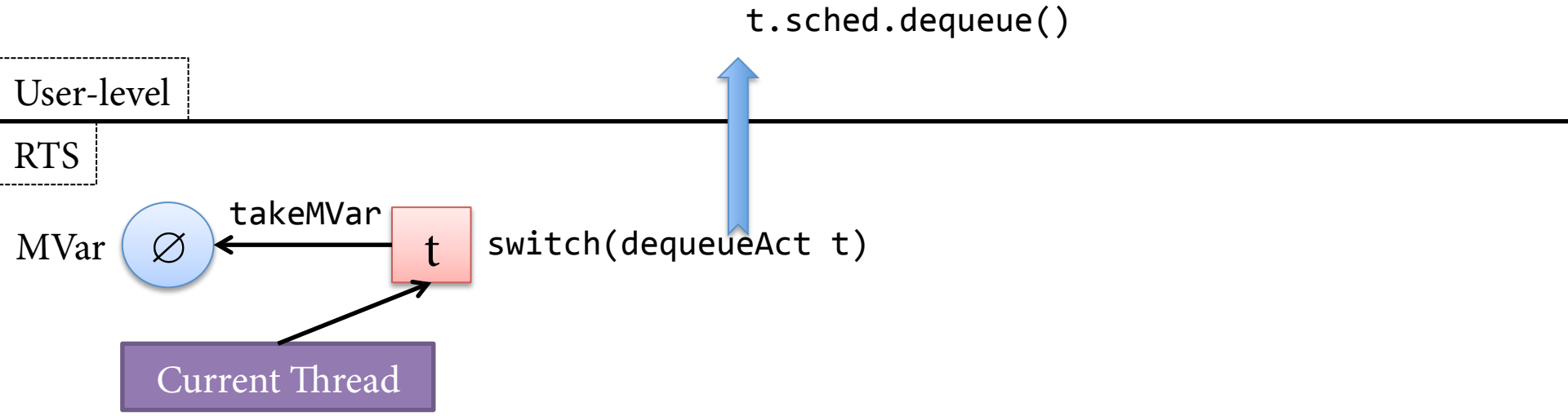

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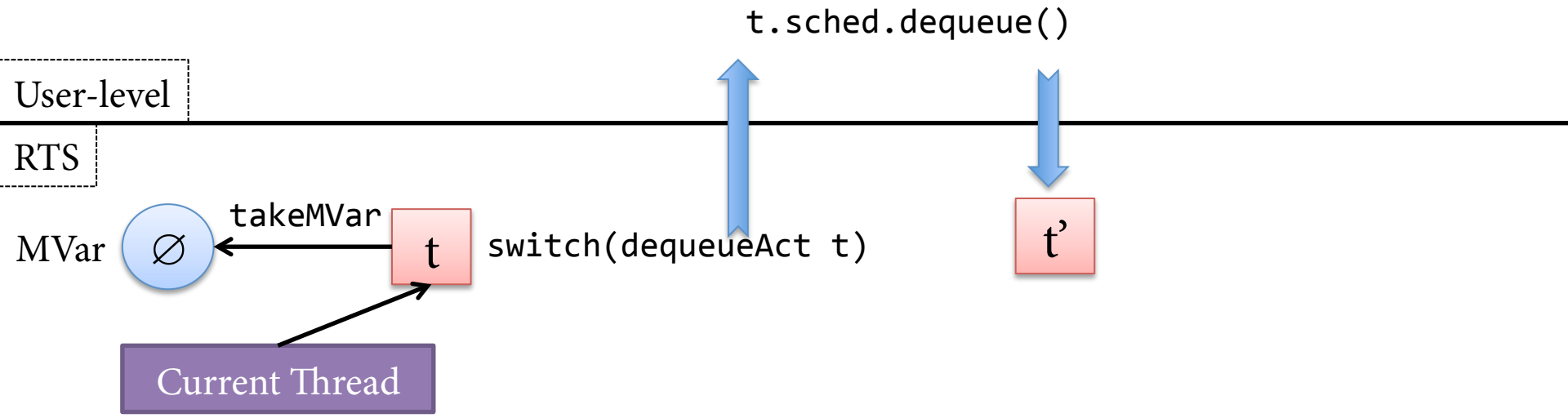

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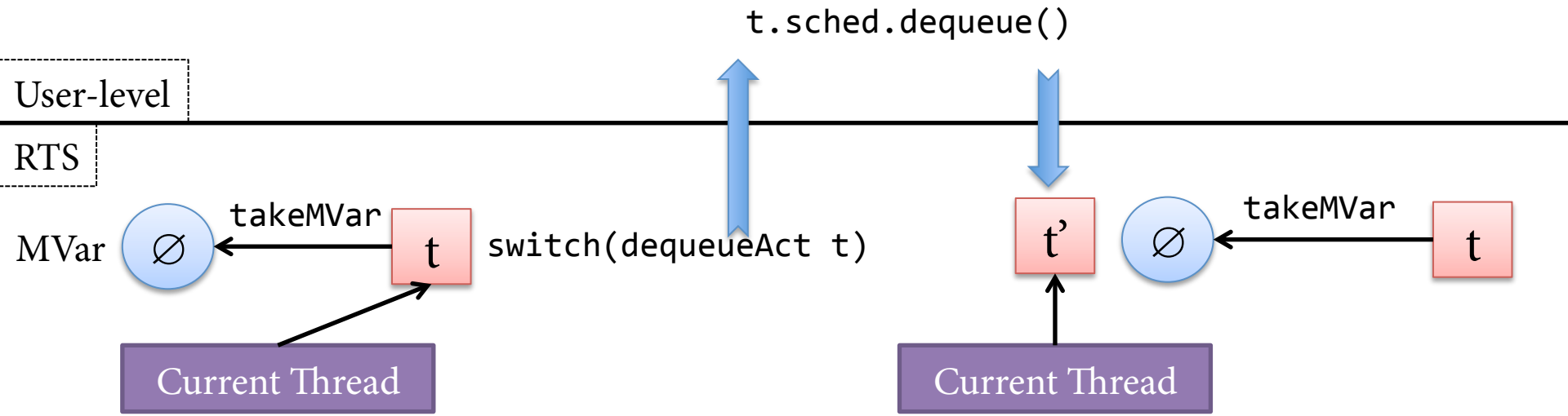
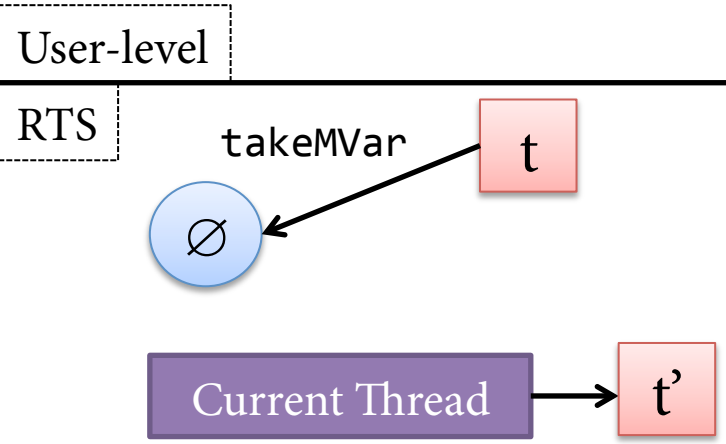
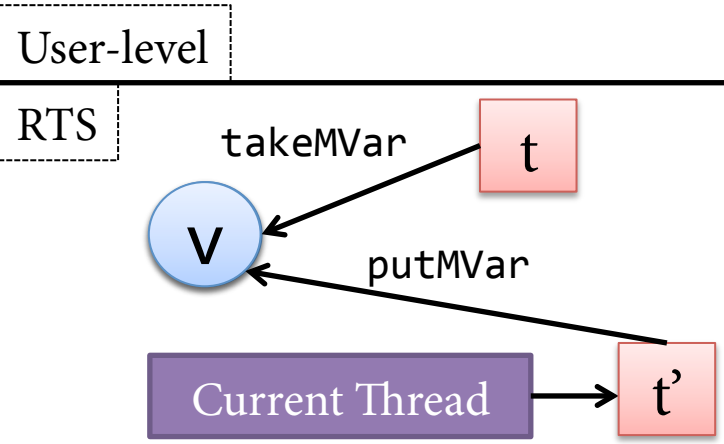


RTS Interaction - Unblocking



RTS Interaction - Unblocking



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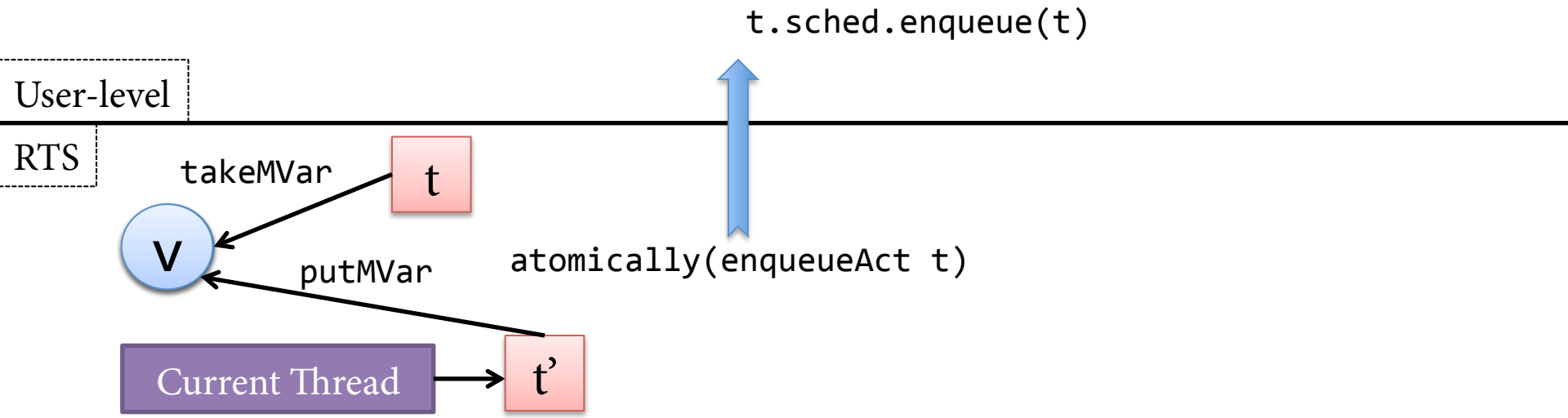

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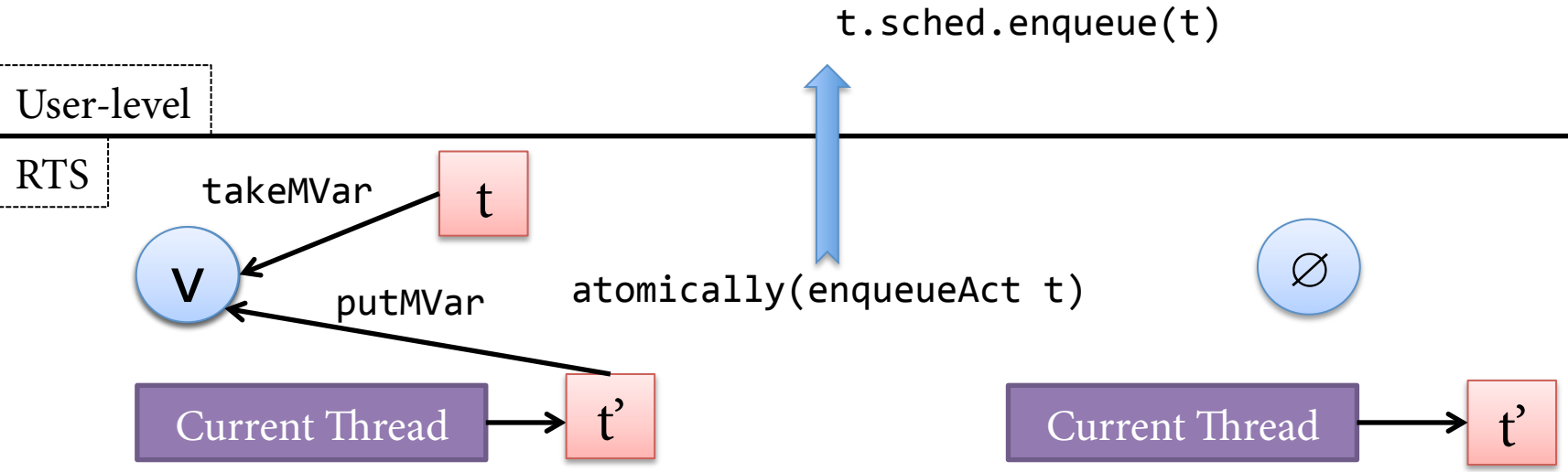

Multicore capable, preemptive, round-robin work-sharing scheduler

```
newtype Sched = Sched (Array Int (TVar[SCont]))

dequeueActivation:: Sched -> SCont -> STM SCont
dequeueActivation (Sched pa) _ = do
  cc <- getCurrentHEC -- get current HEC number
  l <- readTVar $ pa!cc
  case l of
    [] -> retry
    x:tl -> do
      writeTVar (pa!cc) tl
      return x

enqueueActivation:: Sched -> SCont -> STM ()
enqueueActivation (Sched pa) sc = do
  dyn <- getAux sc
  let (hec::Int, _::TVar Int) = fromJust $
       fromDynamic dyn
  l <- readTVar $ pa!hec
  writeTVar (pa!hec) $ l++[sc]
```

```
newScheduler :: IO ()
newScheduler = do
  -- Initialise Auxiliary state
  switch $ \s -> do
    counter <- newTVar (0::Int)
    setAux s $ toDyn $ (0::Int,counter)
    return s
  -- Allocate scheduler
  nc <- getNumHECs
  sched <- (Sched . listArray (0,nc-1)) <$>
           replicateM n (newTVar [])
  -- Initialise activations
  setDequeueAct s $ dequeueActivation sched
  setEnqueueAct s $ enqueueActivation sched

newHEC :: IO ()
newHEC = do
 -- Initial task
 s <- newSCont $ switch dequeueAct
 -- Run in parallel
 runOnIdleHEC s
```

```
forkIO :: IO () -> IO SCont
forkIO task = do
  numHECs <- getNumHECs
  -- epilogue: Switch to next thread
  newSC <- newSCont (task >> switch dequeueAct)
  -- Create and initialise new Aux state
  switch $ \s -> do
    dyn <- getAux s
    let (_::Int, t::TVar Int) = fromJust $
         fromDynamic dyn
    nextHEC <- readTVar t
    writeTVar t $ (nextHEC + 1) `mod` numHECs
    setAux newSC $ toDyn (nextHEC, t)
    return s
  -- Add new thread to scheduler
  atomically $ enqueueAct newSC
  return newSC

yield :: IO ()
yield = switch (\s -> enqueueAct s >> dequeueAct s)
```

Multicore capable, preemptive, round-robin work-sharing scheduler

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newHEC :: IO ()
newHEC = do
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 -- Run in parallel
 runOnIdleHEC s
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yield = switch (\s -> enqueueAct s >> dequeueAct s)
```
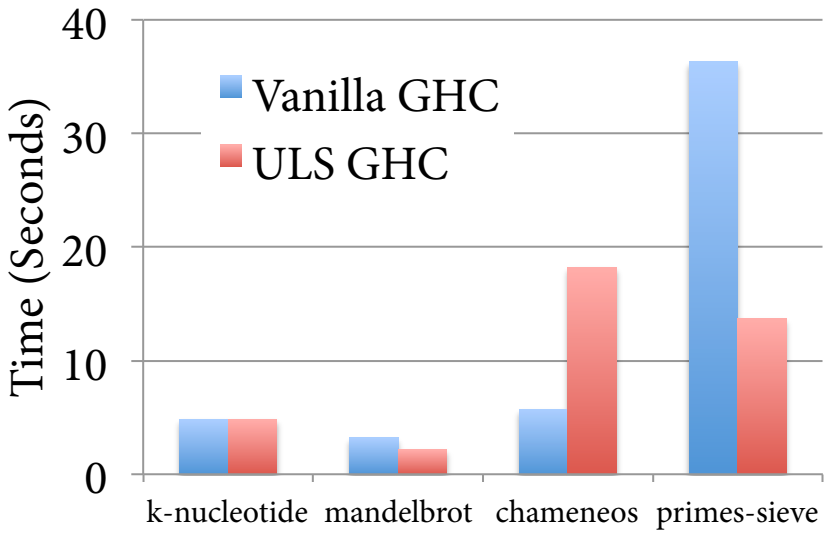
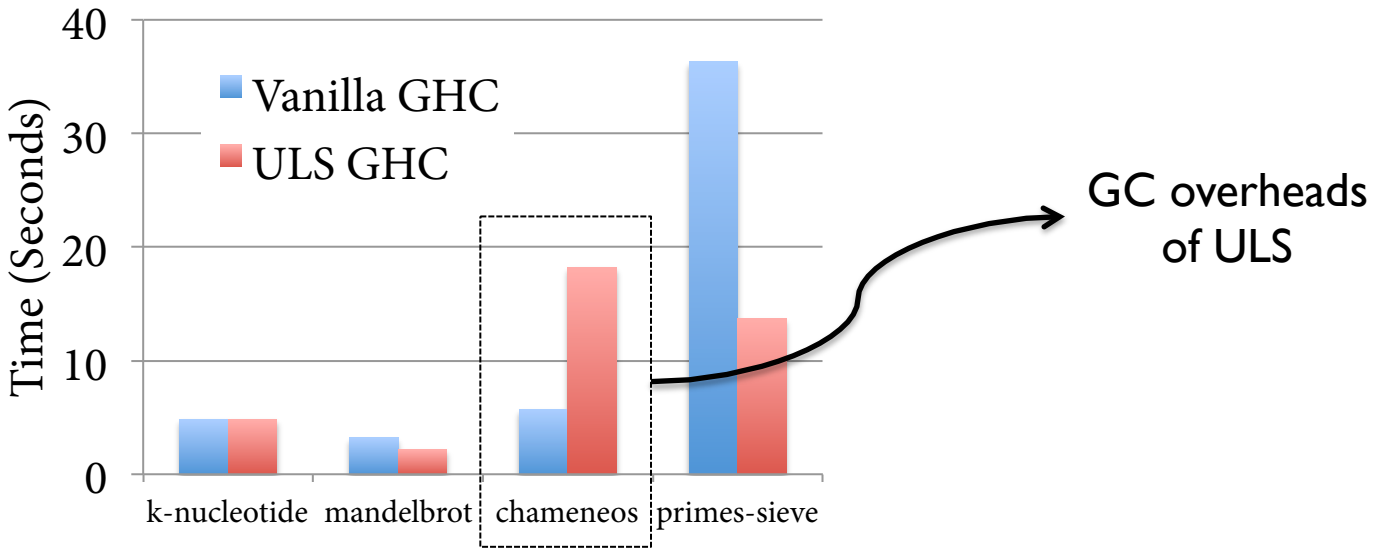



Multicore capable, preemptive, round-robin work-sharing scheduler

```
newtype Sched = Sched (Array Int (TVar[SCont]))

dequeueActivation:: Sched -> SCont -> STM SCont
dequeueActivation (Sched pa) _ = do
  cc <- getCurrentHEC -- get current HEC number
  l <- readTVar $ pa!cc
  case l of
    [] -> retry
    x:tl -> do
      writeTVar (pa!cc) tl
      return x

enqueueActivation:: Sched -> SCont -> STM ()
enqueueActivation (Sched pa) sc = do
  dyn <- getAux sc
  let (hec::Int, _::TVar Int) = fromJust $
       fromDynamic dyn
  l <- readTVar $ pa!hec
  writeTVar (pa!hec) $ l++[sc]
```

```
newScheduler :: IO ()
newScheduler = do
  -- Initialise Auxiliary state
  switch $ \s -> do
    counter <- newTVar (0::Int)
    setAux s $ toDyn $ (0::Int,counter)
    return s
  -- Allocate scheduler
  nc <- getNumHECs
  sched <- (Sched . listArray (0,nc-1)) <$>
           replicateM n (newTVar [])
  -- Initialise activations
  setDequeueAct s $ dequeueActivation sched
  setEnqueueAct s $ enqueueActivation sched

newHEC :: IO ()
newHEC = do
 -- Initial task
 s <- newSCont $ switch dequeueAct
 -- Run in parallel
 runOnIdleHEC s
```

```
forkIO :: IO () -> IO SCont
forkIO task = do
  numHECs <- getNumHECs
  -- epilogue: Switch to next thread
  newSC <- newSCont (task >> switch dequeueAct)
  -- Create and initialise new Aux state
  switch $ \s -> do
    dyn <- getAux s
    let (_::Int, t::TVar Int) = fromJust $
         fromDynamic dyn
    nextHEC <- readTVar t
    writeTVar t $ (nextHEC + 1) `mod` numHECs
    setAux newSC $ toDyn (nextHEC, t)
    return s
  -- Add new thread to scheduler
  atomically $ enqueueAct newSC
  return newSC

yield :: IO ()
yield = switch (\s -> enqueueAct s >> dequeueAct s)
```



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    nextHEC <- readTVar t
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    setAux newSC $ toDyn (nextHEC, t)
    return s
  -- Add new thread to scheduler
  atomically $ enqueueAct newSC
  return newSC

yield :: IO ()
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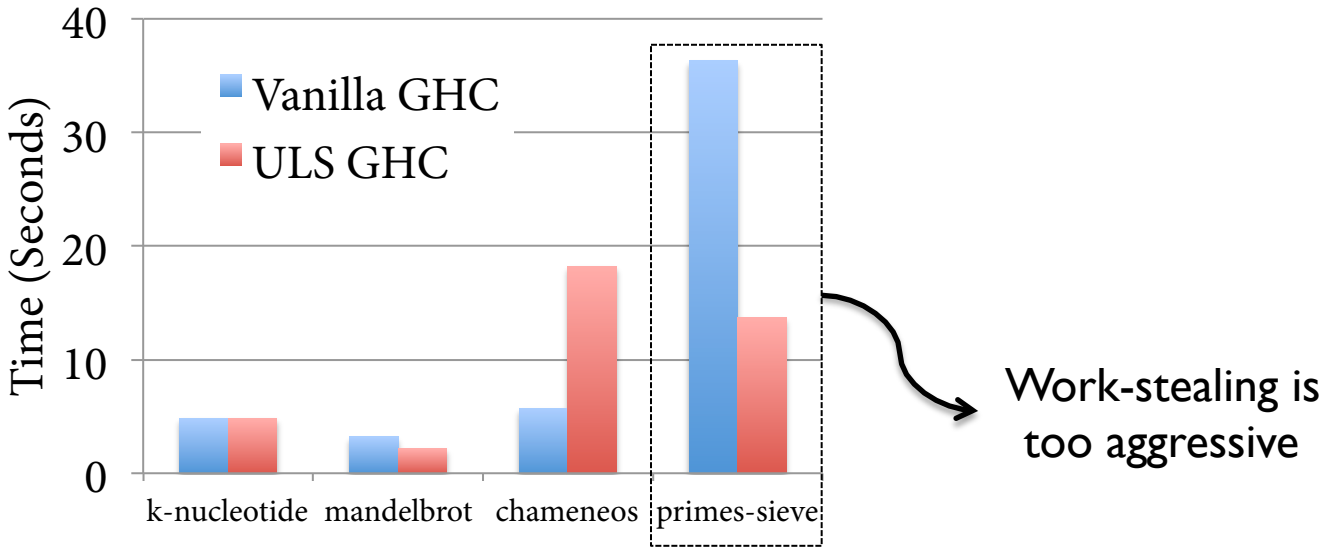

Formalization

Concurrency Substrate

$$x, y \in Variable \quad r, s, \in Name$$

$$
\begin{array}{lcl}
Md & ::= & \mathsf{return}\ M \mid M \gg\!= N \\
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Term

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$$
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Upcalls from the RTS

Dequeue upcall instantiation $\quad H; \Theta \overset{deq}{\hookrightarrow} H'; \Theta'$

(UpDequeue)

$$\frac{s'\ \mathsf{fresh} \quad r\ \mathsf{fresh} \quad D' = (\mathsf{deq}(D), \mathsf{enq}(D), r) \quad M' = \mathsf{switch}\ (\lambda x.\, \mathsf{deq}(D)\ s) \quad \Theta' = \Theta[s \mapsto (M, D)][r \mapsto \mathsf{toDyn}\ ()]}{\langle s, M, D \rangle; \Theta \overset{deq}{\hookrightarrow} \langle s', M', D' \rangle; \Theta'}$$

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(UpEnqueueRunning)

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Formalization

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 & \mid & \mathsf{atomically}\ M \mid \mathsf{retry} \\
Sc & ::= & \mathsf{newSCont}\ M \mid \mathsf{switch}\ M \mid \mathsf{runOnIdleHEC}\ s \\
Sls & ::= & \mathsf{getAux}\ s \mid \mathsf{setAux}\ s\ M \\
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\end{array}
$$

Term

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Upcalls from the RTS

Dequeue upcall instantiation $H; \Theta \overset{deq}{\hookrightarrow} H'; \Theta'$

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IO

E[M] tick **E[yield >> M]**

Formalization

Concurrency Substrate

$$x, y \in Variable \quad r, s, \in Name$$

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IO

`E[M]` → tick → `E[yield >> M]`

atomically STM

`E[atomically(P[M])]` → tick → Suspend transaction and switch

Formalization

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Upcalls from the RTS

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IO

atomically STM

Switch STM

`E[M]` → tick → `E[yield >> M]`

`E[atomically(P[M])]` → tick → Suspend transaction and switch

`E[switch(P[M])]` → tick

Formalization

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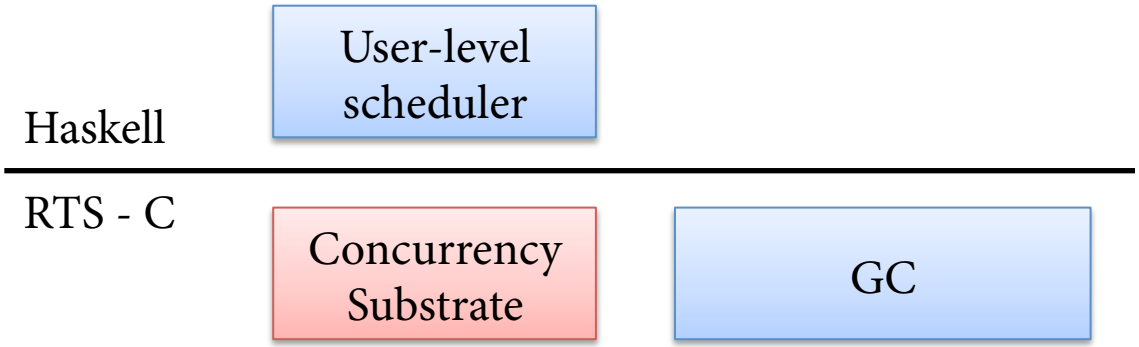
atomically STM

`E[atomically(P[M])]` → tick → Suspend transaction and switch

Switch STM

`E[switch(P[M])]` → tick → *Disable Interrupts!*

Future directions



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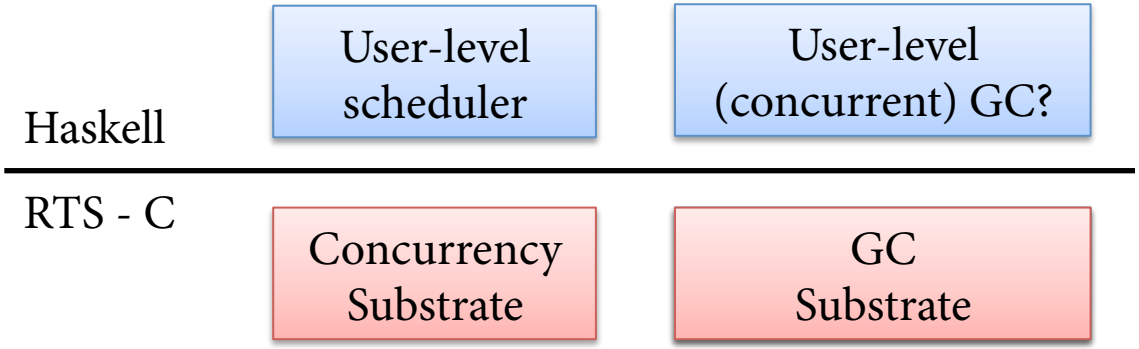

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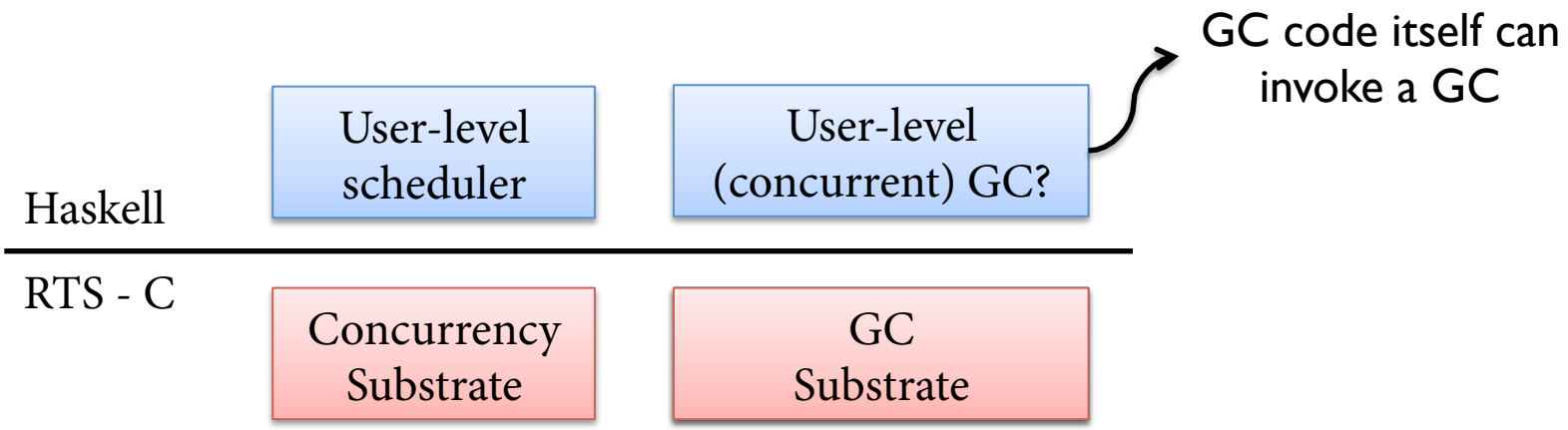

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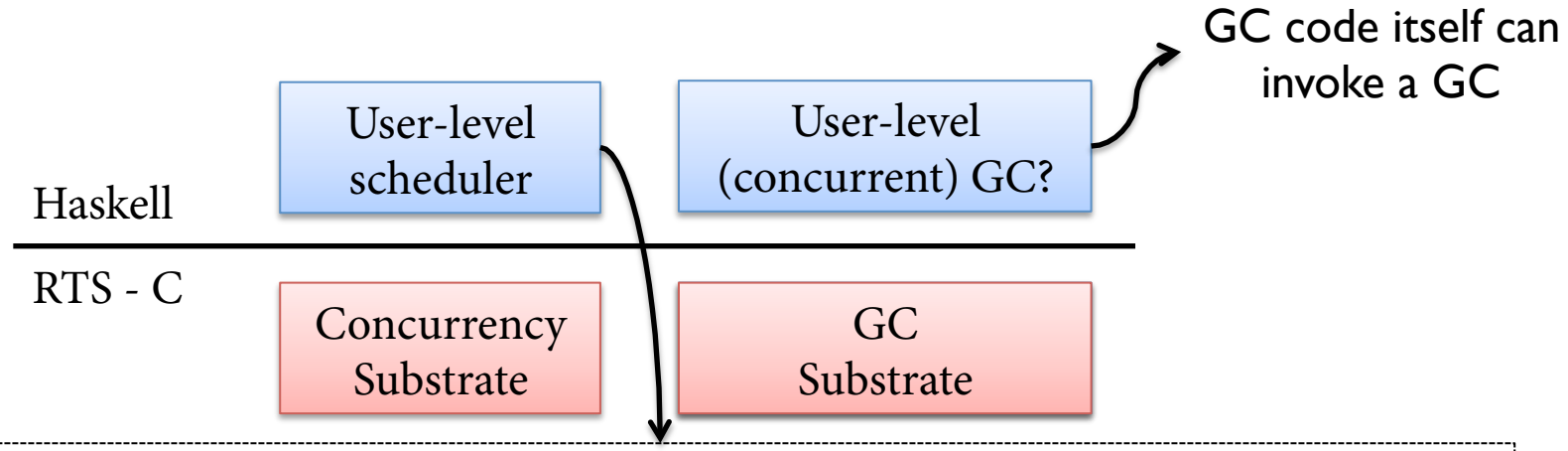

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  - Correct Scheduler ⇒ Each thread runs as if given its own processor and register set
  - Scheduler access under STM ⇒ Treat scheduler as sequential process

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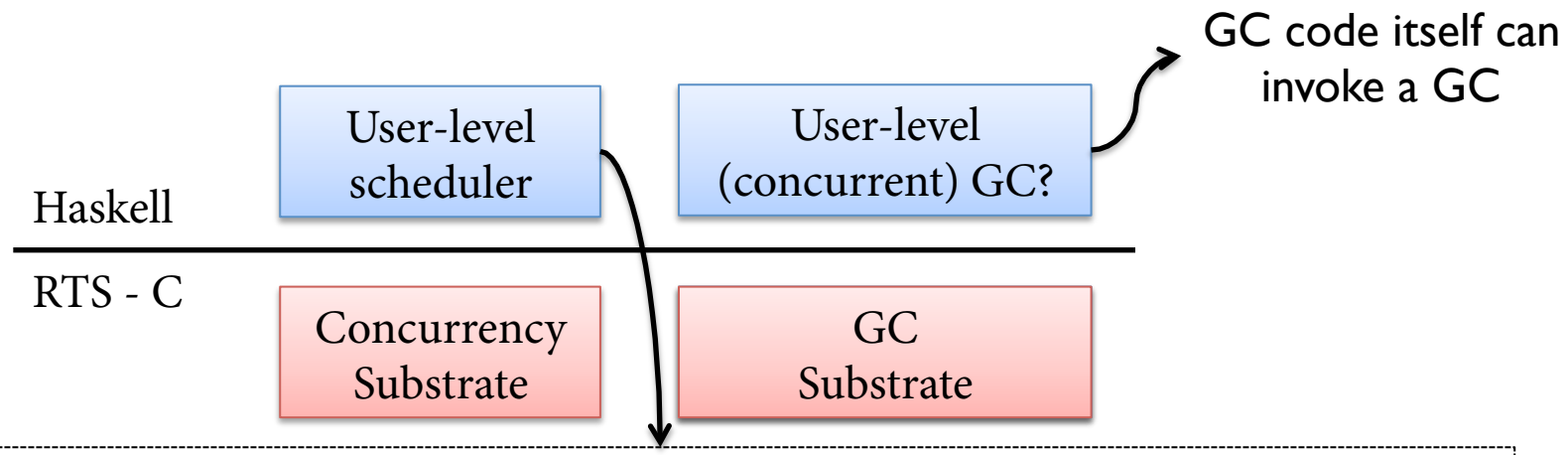

- Verifying the functional correctness of schedulers
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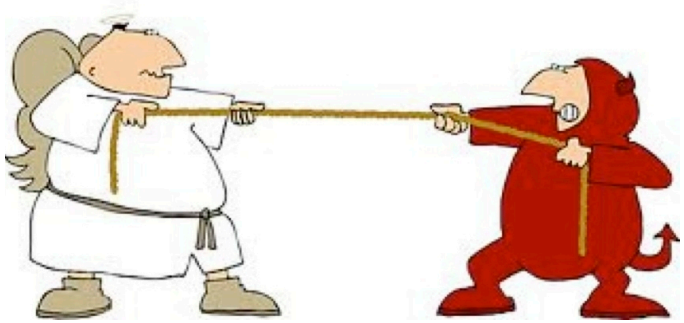
  - Scheduler access under STM ⇒ Treat scheduler as sequential process

- FP abstractions for eventually consistent systems
  - Operations on ECDTs described as pure functions over axiomatic executions
  - A relational specification language for specifying consistency assertions over axiomatic executions

Conclusion



- Functional programming abstractions simplify concurrent programming
  - Rx-CML: Synchronous communication over geo-distributed systems
  - Concurrency Substrate: Scheduler activation + STM for writing schedulers
- Abstractions introduce indirection resulting in overheads
  - Rx-CML slower than explicit async under contention
  - Conc. Subs: Scheduler allocations increase GC overheads